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PECVD SiN_x passivation with more than 8 MV/cm breakdown strength for GaN-on-Si wafer stress management☆

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In this work, multi-layer PECVD SiN_x/SiN_x and SiN_x/SiO_y passivations are developed featuring very high soft breakdown strength and tunable stress properties, which would allow for stress engineering and wafer bow minimization. AlGaN/GaN-on-Si wafers (150 mm) with very low initial bow (< 5 µm) are processed in a CMOS compatible manner. The effect of the major processing steps, namely passivation and metal deposition, on the wafer bow is continuously monitored. In this process aimed at power devices, relatively thick passivation is needed (1.5 µm), which would induce very high stresses on the wafer if a single-layer deposition is applied. Hence, deposition of multiple layers is explored through mechanical modelling and simulation, leading to a stress-free passivation. The optimized multi-layer dielectric consists of two different SiN_x single layers (referred to as T40 and R100), which have opposite stress properties, with T40 being tensile and R100 being compressive. By adjusting the thickness ratio of both layers and the number of total layers, mechanical stress within the multi-layer can be neutralized to achieve stress-free deposition. In addition, the optimization of the film properties includes the electrical properties of the passivation, and is designed primarily for high voltage applications. The developed SiN_x/SiN_x passivation has a soft breakdown strength with more than 8 MV/cm, and leakage currents below 1 nA/mm^2 up to soft breakdown. After dielectric development, Schottky and MIS device characteristics with SiN_x/SiN_x multi-layers are characterized in DC and pulse mode measurements. As measurements suggest, the developed passivation is suitable for GaN-on-Si HEMT applications.

1. Introduction

Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) have raised large industrial interest worldwide over the last two decades. The increased commercial adoption of GaN HEMTs for high voltage and MEMS applications (Amano et al., 2018; Chen et al., 2017) is driven by the availability of large diameter GaN-on-Si wafers, which could be processed in cost-effective CMOS processing lines. Despite the high lattice and thermal mismatch between GaN and Si, wafers with very low initial bow values are available due to stress compensation in epitaxial growth. However, since in power device fabrication, many layers of relatively thick passivation and thick metallization are needed, excessive wafer bow seems unavoidable using common CMOS compatible processing. The wafer bow causes technological difficulty in photolithography, and the residual stress can lead to degraded device performance and to initiation of wafer mechanical defects and even cracks. This can lead to reduced epi-wafer quality and functional device yield. The thick layers required for high-voltage passivation are a major source of wafer stress and bow. While the initial thin passivation can be Low-Pressure Chemical Vapor Deposition (LPCVD) based, all subsequent passivation layer depositions has to rely on Plasma-Enhanced Chemical Vapor Deposition (PECVD). Such films usually vary in electrical and mechanical properties, depending on the details of the deposition process, so that single layer films have distinctively different mechanical and electrical properties from wafer to wafer. In this work, the optimization procedure as well as modelling and film properties of a

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stress-compensated high-voltage compatible PECVD dielectric will be addressed and the process related properties, such as etch rate and film uniformity, will be discussed. The experiments were executed on AlGaN/GaN-on-Si and wet (w) SiO_2/Si wafers with a diameter of 150 mm.

The starting point for this work are N-rich PECVD SiN_x (R-, S- and T-series) and PECVD SiO_y (O-Series) layers with different electrical, optical and mechanical properties depending on gas mixture, process pressure and plasma power (Fig. 1). The films are named according to the recipe and the chosen plasma power during deposition in W. To increase the total soft dielectric breakdown strength (E_{bs}), a multi-layer approach (Ahammou et al., 2022; Chen, Tsai, & Yang, 2021; Feng et al., 2021; Gefle, Lebedev, & Uschakov, 1997; Hanby et al., 2019) was chosen. All PECVD depositions within this work were done in a Oxford Instruments PlasmaPro NGP80 PECVD reactor with process settings according to Table 1.

Since high-power dielectrics need relatively high thicknesses to block high voltages, stress management becomes important to allow for good film quality without cracking or buckling and processability after deposition. When a film with high intrinsic stress is chosen, the wafer is subject to bending, as shown in Fig. 2. The top row (Fig. 2(a)–(c)) show the reference wafers before deposition with small warpage. After PECVD deposition of 1350 nm T40, the wafer shows a high concave bow of 95 μm (Fig. 2(d)), while 950 nm R100 result in a convex bow of − 115 μm (Fig. 2(e)). 2400 nm O40 leads to a bow of − 112 μm (Fig. 2(f)). The bow direction of the wafer allows for interpretation of the layer stress. A film leading to bowl-shaped or concave warpage has tensile stress, while compressive layers lead to convex warpage. The deposited multi-layers either consisted of T40/R100 pairs for SiN_x/SiN_x multi-layers or T40/O40 pairs in the case of SiN_x/SiO_y multi-layers. These films were chosen due to their E_{bs} value and opposite stresses. This allows not only the deposition of intrinsically stress-neutral multi-layers, but also stress-engineering and active bow compensation.

With knowledge about the intrinsic stress parameters of the individual films, simulative optimization of T40/R100 and T40/O40 multi-layers in terms of total stress is done to find a suitable set of deposition parameters in the following.

The films are electrically characterized with Metal-Insulator-Metal (MIM) capacitors to extract dielectric breakdown behaviour and leakage currents at different thicknesses.

2. Bow and stress measurement

The wafer bow was extracted using tactile needle scanning on a Veeco DEKTAK 8 stylus profilometer. For accurate measurement a total of eight scans at equidistant angles were done over a diameter of 140 mm. The raw scan data of pre-bow and post-bow were subtracted and the bow difference was fitted to a polynomial of 4th grade. The resulting fitting equation allowed the calculation of the wafer curvature (R), which is directly dependent on the film stress (σ_f). The higher the thermal mismatch between substrate and deposited films, the higher the resulting stress and consecutively, the higher the resulting wafer bow. The correlation between R and σ_f is given in Stoney's equation (Janssen, Abdalla, van Keulen, Pujada, & van Venrooy, 2009; Schwarzer & Richter, 2006):

$$\sigma_f = \frac{Y_s^{'} t_s^2}{6 t_f R}, \tag{1}$$

where t_f is the film thickness. In the case of a single film deposition on the wafer top-side it is $\sigma_i = \sigma_f$. Stress-wise, the multi-layer is treated as a single layer since all layers building up the stack are deposited in a single PECVD process. For the measured stress it therefore is $\sigma_{ML} = \sigma_f$.

For stress optimization, 675 μm thick $Si_{[100]}$ substrates were used. Before deposition of the dielectric films, a wet thermal oxidation was done to obtain 1 μm w-SiO_2 on both substrate sides as insulating surface passivation. This substrate type is referred to as w-SiO_2/Si wafers in the following. The w-SiO_2 allows closer resemblance of the thermal isolation of a GaN-on-Si wafer. Therefore the depositions are transferable to 1000 μm thick GaN-on-Si wafers. The AlGaN/GaN-on-Si epitaxy wafers within this work were provided by AIXTRON SE. Depositions on latter wafers were done at a stage, where HEMT devices were already produced as described later. After each deposition step, film thicknesses were measured using a ProMicron NanoCalc-2000 white light reflectometer.

For visualization of wafer warpage, the raw scan data was post-processed to remove the wafer tilt and fitted with a surface plot. The surface is shown in the topography maps of the wafer warpage.

3. Stress-engineering of SiN_x/SiN_x and SiN_x/SiO_y multi-layers

3.1. Simulation of stress distribution

Optimization of a multi-layered dielectric relies on precise knowledge of the deposition process itself, the resulting film properties as well as the substrate properties. Since GaN-on-Si wafers are grown with several epitaxial layers, the substrate already is a complex system with initial stress and warpage. In order to calculate the effects of multi-layered dielectrics, a simulation routine (Hsueh, Luttrell, & Cui, 2006; Kim & Paik, 1999; Klein, 2000) was implemented to account for multiple heating, cooling and deposition steps of layers with different properties on top or bottom of a substrate as depicted in Fig. 3.

The wafer system consists of n top-side layers ($_i$), m back-side layers ($_j$) and the substrate ($_s$). The coordinate system is located at the top-side of the substrate and is denoted as $z = 0$. During the k process steps (l), the system is subject to different temperature changes $\Delta T(l) = T_{end}(l) - T_{start}(l)$. Depending on the process, $\Delta T(h)$ describes either heating ($+\Delta T(h)$) or cooling ($-\Delta T(l)$) and indicates whether a deposition or temperature transition is being executed. The expansion or shrinking of the individual layers leads to stress due to thermal mismatch. The system remains under stress after cooling down to room temperature at the end of each deposition step. It is assumed that all stresses are elastic and that there is no stress relaxation during heating and cooling or additional stresses from lattice mismatch. The stress of the top-side layers ($\sigma_i(l)$), the substrate ($\sigma_s(l)$) and the back-side layers ($\sigma_j(l)$) is calculated after each step as follows (Hsueh et al., 2006):

$$\sigma_i(l) = Y_i^{'}\left(c + \frac{z_i - b}{r} - \alpha_i \Delta T(l)\right) + \sigma_r|_{0 \le l \le k,\ 1 \le i \le n} \tag{2}$$

$$\sigma_s(l) = Y_s^{'}\left(c + \frac{z_s - b}{r} - \alpha_s \Delta T(l)\right) + \sigma_r|_{0 \le l \le k} \tag{3}$$

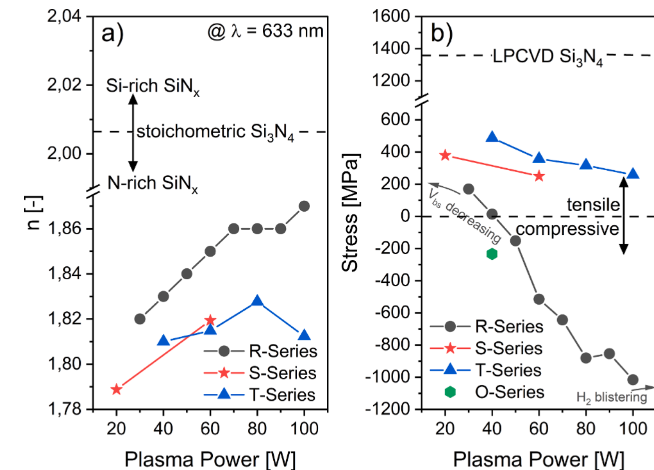

Fig. 1. Refractive index (a) and film stress (b) of different N-rich SiN_x and SiO_y recipes as function of plasma power.

Table 1
SiN_x and SiO_y deposition recipes.

Film	Temp. [°C]	Press. [mTorr]	HF [W]	SiH_4 [sccm]	NH_3 [sccm]	N_2 [sccm]	N_2O [sccm]	D $\left[\frac{nm}{min}\right]$
R(y)	350	1000	y	1	20	980	0	8.0
S(y)	350	1000	y	5	50	1975	0	22.0
T(y)	350	1350	y	5	50	1975	0	24.5
O(y)	350	800	y	5	0	0	510	58.0

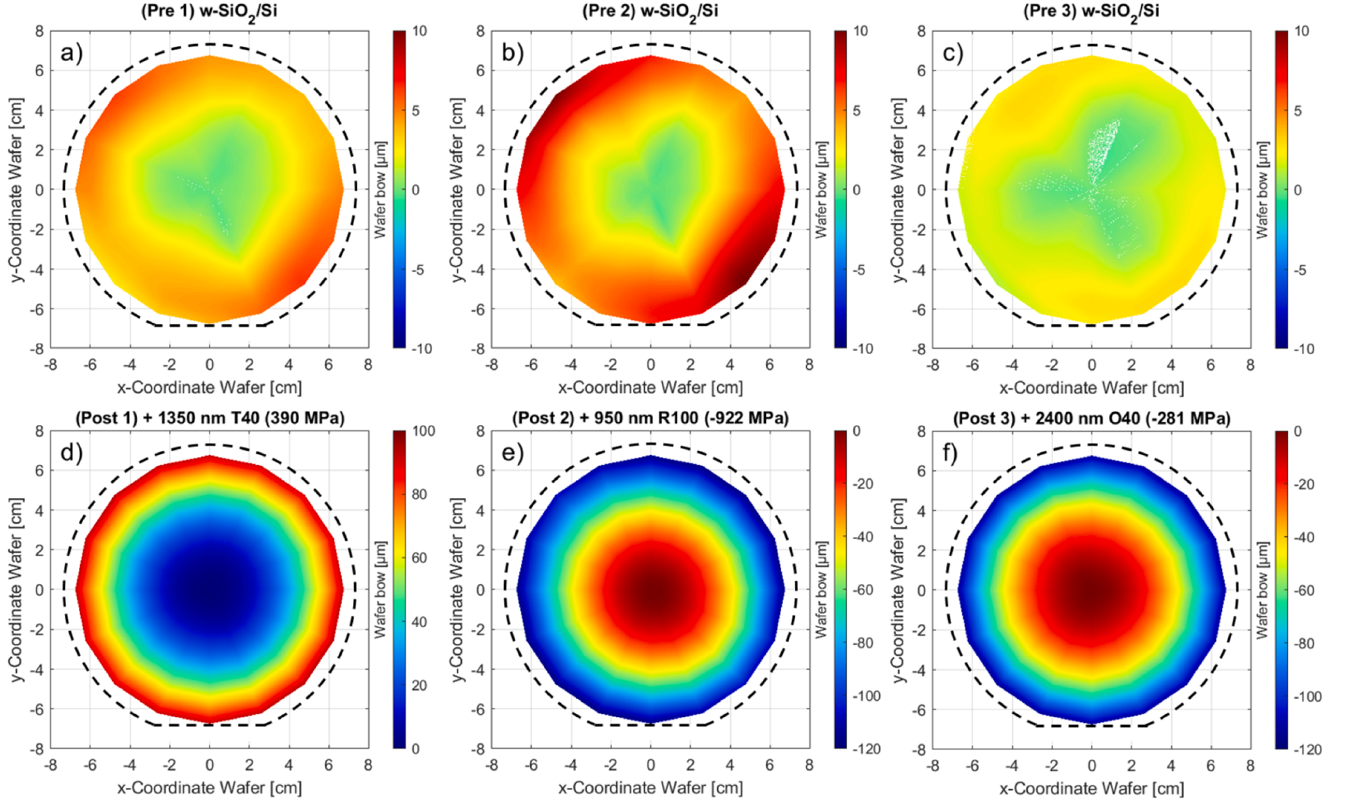

Fig. 2. Measured wafer bow of 150 mm w-SiO_2/Si substrates before (a)–(c) and after (d)–(f) single layer T40, R100 and O40 PECVD deposition. T40 leads to bowl-shaped or concave warpage, R100 and O40 lead to convex warpage of the wafer. The resulting bows are high due to high layer thicknesses and stresses.

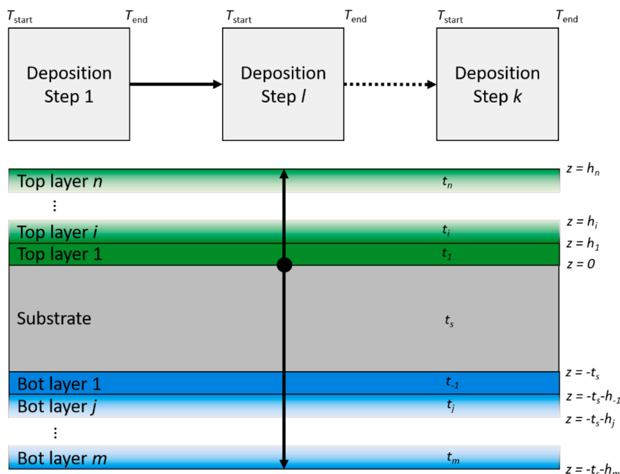

Fig. 3. Schematic process flow and cross-section of front-side and back-side layer deposition on a substrate with corresponding coordinate system and parameters.

$$\sigma_j(l) = Y_j'\left(c + \frac{z_j - b}{r} - \alpha_j \Delta T(l)\right) + \sigma_r|_{0\le l\le k,\ 1\le j\le m} \tag{4}$$

with $Y' = Y/(1-\nu)$ as the biaxial modulus, Young's modulus (Y), Poisson's ratio (ν), height (z), coefficient of thermal expansion (α) and residual stress from PECVD deposition (σ_r). The parameters that were used in the stress simulation are given in Table 2. The three stress parameters (c, b and r) are obtained from Hsueh et al. (2006)

$$c = \frac{\left(Y_s' t_s \alpha_s + \sum_{i=1}^{n} Y_i' t_i \alpha_i + \sum_{j=1}^{m} Y_j' t_j \alpha_j\right)\Delta T(h)}{Y_s' t_s + \sum_{i=1}^{n} Y_i' t_i + \sum_{j=1}^{m} Y_j' t_j}, \tag{5}$$

$$b = \frac{-Y_s' t_s^2 + \gamma_t + \gamma_b}{2\left(Y_s' t_s + \sum_{i=1}^{n} Y_i' t_i + \sum_{j=1}^{m} Y_j' t_j\right)}, \tag{6}$$

$$\frac{1}{r} = \frac{3\left(Y_s'(c - \alpha_s \Delta T(h)) t_s^2 - \delta_t - \delta_b\right)}{Y_s' t_s^2 (2t_s + 3b) + \xi_t + \xi_b}, \tag{7}$$

where t is the layer thickness. The sum parameters (γ, δ, ξ) summarize different terms of top-side ($_t$) and back-side ($_b$) layers and are calculated

Table 2
Substrate and layer properties.

Material	Y [GPa]	ν [−]	Y' [GPa]	α $\left[\frac{10^{-6}}{K}\right]$	σ_r [MPa]	t [μm]
$Si_{[100]}$ [a]	130	0.28	234.4	3.79	0	675
$Si_{[111]}$ [a]	169	0.18	254.1	3.79	0	675
w-SiO_2 [b]	57	0.17	68.7	1.60	0	1
O40 [b]	57	0.17	68.7	1.60	− 185.5	var.
R100 [c]	310	0.55	688.9	2.12	− 599.1	var.
T40 [c]	235	0.30	335.7	4.60	780.6	var.
GaN [d]	324	0.33	481.5	5.60	0	var.
AlN [e]	345	0.32	508.6	4.15	0	var.

[a] Calc. Hopcroft et al. (2010).
[b] Calc. Petersen (1978).
[c] Extrap. Gan et al. (2018).
[d] Calc. Ambacher et al. (2002); Lalinsk et al. (2012); Qin et al. (2017).
[e] Calc. Ambacher et al. (2002); McNeil et al. (1993).

according to Hsueh et al. (2006)

$$\gamma_t = \sum\nolimits_{i=1}^{n} Y_i' t_i (2h_{i-1} + t_i), \tag{8}$$

$$\gamma_b = \sum\nolimits_{j=1}^{m} Y_j' t_j (2h_{j-1} + t_j), \tag{9}$$

$$\delta_t = \sum\nolimits_{i=1}^{n} Y_i' t_i (c - \alpha_i \Delta T)(2h_{i-1} + t_i), \tag{10}$$

$$\delta_b = \sum\nolimits_{j=1}^{m} Y_j' t_j (c - \alpha_j \Delta T)(2h_{j-1} + t_j), \tag{11}$$

$$\xi_t = \sum_{i=1}^{n} Y_i' t_i \left(6h_{i-1}^2 + 6h_{i-1} t_i + 2t_i^2 - 3b(2h_{i-1} + t_i)\right), \tag{12}$$

$$\xi_b = \sum_{j=1}^{n} Y_j' t_j \left(6h_{j-1}^2 + 6h_{j-1} t_j + 2t_j^2 - 3b(2h_{j-1} + t_j)\right). \tag{13}$$

If the stressed system is non-symmetric, i.e. different numbers, materials or thicknesses of layers on the frontside and back-side, the wafer will bend. The resulting R depends primarily on the thermal mismatch of the layers and the substrate and can be described using multi-layer-modified Stoney's equation (Kim & Paik, 1999):

$$\frac{1}{R} = \frac{6\sum_{l=1}^{k}\left(\sum_{i=1}^{n} t_i \sigma_i(l) - \sum_{j=1}^{m} t_j \sigma_j(l)\right)}{Y_s' t_s^2}, \tag{14}$$

The maximum bow (w_s) is obtained by considering the geometry of the curvature and the size of the substrate (L_s). It is located at the edges of the wafer and is calculated according to Kim & Paik (1999)

$$w_s = \frac{L_s^2}{8R}. \tag{15}$$

In this work we investigated wafers with 150 mm diameter. However, the final bow is calculated only within a diameter of 140 mm due to measurement setup limitations of the tactile profilometer.

In order to qualify the multi-layer, the thickness of the individual layers (t_{l1} and t_{l2}) are summarized for the total thickness (t_{ML}):

$$t_{ML} = N(t_{l1} + t_{l2}) = N t_{l2}(1 + \beta), \tag{16}$$

where N is the total number of layer-pairs of the multi-layer and $\beta = d_{l1}/d_{l2}$ is the layer thickness ratio. The resulting multi-layer stress (σ_{ML}) then follows to Kim & Paik (1999):

$$\sigma_{ML} = \frac{4Y_s' t_s w_s}{3L_s^2 t_{ML}}. \tag{17}$$

The aim of the multi-layer was to generate an intrinsically stress-neutral stack to avoid high changes in wafer bow when thick dielectrics are deposited. However, a net stress can also be generated intentionally by adjusting β. This allows bow correction of already warped wafers to minimize the bow.

Fig. 4 shows the simulation of an exemplary process flow of wet thermal oxidation of a Si substrate, followed by T40/R100 multi-layer PECVD deposition at 350 °C. The top, middle and bottom row of Fig. 4 depict the top layers, substrate and bottom layers of the wafer system in cross-section, respectively. The simulation was done with material properties as listed in Table 2. The properties of T40 and R100 were fitted to measured data (Fig. 2) as well as results from Gan, Wang, & Chen (2018). The simulation already shows an optimized 1 μm T40/R100 multi-layer which is intrinsically stress-neutral with a total stress of − 3.15 MPa at $\beta = 1.73$ and $N = 2$.

Blank wafers are assumed to have no bow, i.e. $R = \infty$ and $w_s = 0$ μm. This assumption is valid, since the measurement result only take bow difference into account.

3.2. Multi-layer deposition and verification

Before deposition of multi-layers, single layer T40, R100 and O40 films were investigated and characterized regarding their mechanical properties. In a first step, the film stress was measured after deposition of the respective film on a w-SiO_2/Si substrate. Fig. 5(a) shows measured film stresses of O40, T40 and R100 films at different thicknesses ranging from 5 nm to 2 μm. The mechanical simulation with film parameters from Table 2 is in good agreement with the experimental values and follows the almost linear trend over film thickness. The simulation is shown with the corresponding 95% confidence interval for the respective material. Each film shows a small stress relaxation effect when higher film thicknesses are deposited in a single step. This strain relaxation is − 5% for T40, − 8% for R100 and − 3% for O40 from 5 nm to 2 μm. The mean value of measured stress is 436.82 MPa, − 942.84 MPa and − 243 MPa for T40, R100 and O40, respectively. Since the simulation accounts for the stress relaxation effect, multi-layer simulation is

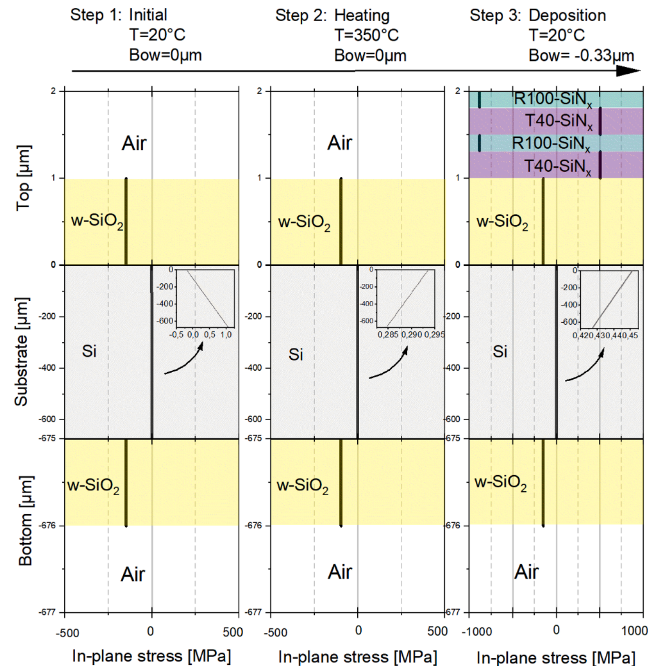

Fig. 4. Simulation of deposition steps during stress optimization on w-SiO_2/Si substrates. At first, w-SiO_2 is deposited and cooled. The substrate is heated to PECVD process temperature and deposition of the multi-layer takes place, followed by cooling to room temperature. The simulation shows an optimized 2NN multi-layer.

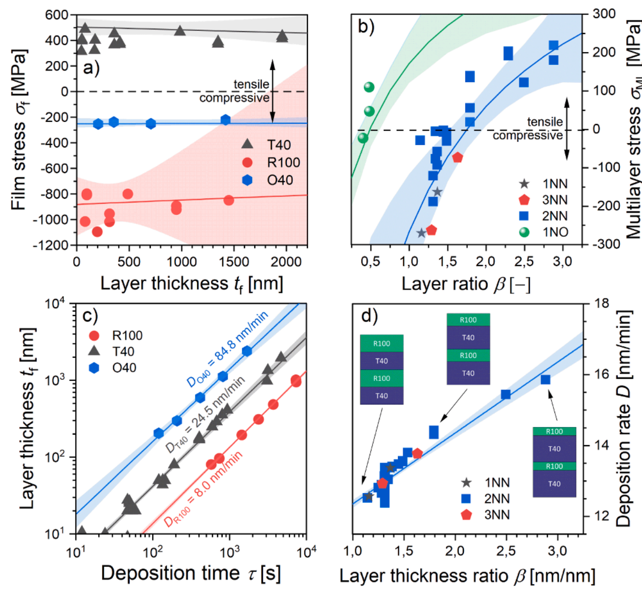

Fig. 5. Measured mechanical layer properties of T40, R100 and O40 (a) at different thicknesses, and 1NN, 2NN, 3NN and 1NO multi-layers (b) at different thickness ratios. The deposited thicknesses (c) of T40, R100 and O40 show a linear correlation with time over a wide range. A linear depedency of the multi-layer thickness with time is visible in (d).

valid over a wide range of thicknesses.

The SiN_x/SiN_x multi-layers were deposited with one (1NN), two (2NN) and three (3NN) layer-pairs, for SiN_x/SiO_y multi-layers only one (1NO) layer-pair was used. Fig. 5(b) shows measured and simulated stress data for all multi-layer types within this work at different β values. The total amount of layers within the multi-layer only affects the simulated stress values slightly, therefore simulated stress and 95% confidence interval for 2NN is shown only. The simulation fits the measured data well and allows for prediction of total multi-layer stress depending on the deposited materials and β. Varying β not only allows deposition of intrinsically stress-neutral multi-layers, but also stress-engineering with a defined resulting stress to actively compensate for wafer bow during processing. It should be noted that β has a non-linear influence on σ_{ML}, the stress-neutral point ($\sigma_{ML} = 0$ MPa) is $\beta = 1.75$ for 2NN and $\beta = 0.45$ for 1NO. Since the deposition rate (D) of O40, T40 and R100 follows a linear scheme over a wide range of thicknesses (Fig. 5 (c)), adjustment of the PECVD deposition time is indepenent of the final layer thickness and allows easy recipe adjustment to obtain the desired stress compensation effect. This is also proven by the fact that the deposition rate of the multi-layer scales linearly with β as shown in Fig. 5 (d) for 1NN, 2NN and 3NN multi-layers within $1.15 \leq \beta \leq 2.9$.

From the initial mechanical film investigation, one substrate with T40, R100 and 2NN multi-layer was stored in clean-room environment at 20 °C for long-term measurements of the mechanical stability. The stress measurements were executed at irregular intervals on the same wafers. The measurements proved, that T40 and R100 films are mechanically stable and do not suffer from creeping stress relaxation as shown in Fig. 6. The 2NN multi-layer also showed no stress relaxation over several weeks.

Wafer maps of the optimized 2NN and 1NO multi-layers are shown in Fig. 7 on w-SiO_2/Si and GaN-on-Si substrates. The top row (Fig. 7(a)–(c)) shows the pre-bow of the substrate before deposition, the bottom row (Fig. 7(d)–(f)) shows the post-bow. The visible roughness comes from pre-processed metal structures on the wafers, that were later used to characterized the dielectric electrically. The optimized 2NN as well as the 1NO multi-layer did not change the total wafer bow and introduced stress within ±30 MPa, despite the high thicknesses of 1.5 µm for 2NN and 800 nm for 1NO. In Fig. 7(b) and (e), the process was successfully

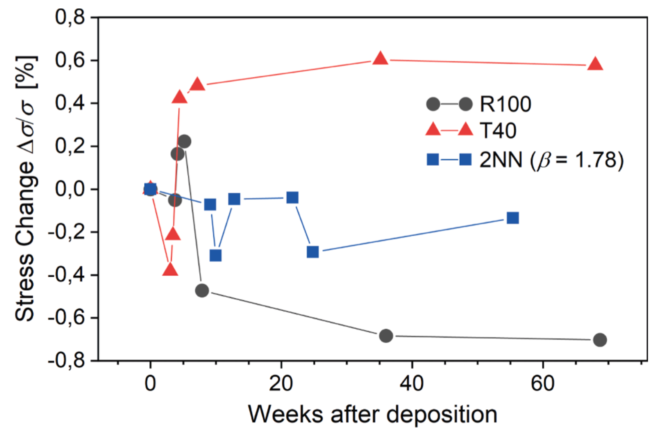

Fig. 6. T40, R100 and 2NN long-term stress measurement.

transferred to a AlGaN/GaN-on-Si substrate with pre-processed HEMT structures.

3.3. Multi-layer etching

After deposition of the 2NN dielectric, usually a via opening needs to be structured to allow interconnection to the lower-level metals using SF_6/Ar-based Reactive Ion Etching (RIE) with resist mask. Fig. 8(a) shows the characteristic plasma spectrum during etching of SiN_x using above mentioned etchant. The predominant spectral lines are specific for the molecules in the chamber, which are SiF_2 (387 nm), F (684 nm and 703 nm) and N_2 (655 nm, 739 nm and 774 nm). During the process, wavelengths 387 nm, 686 nm and 703 nm are monitored as endpoint signals, which is shown in the time plot of Fig. 8(b). All three lines show a characteristic intensity change when either the T40 or R100 film is exposed to the etchant species. Especially the F-line at 703 nm shows a higher intensity during etching of R100 compared to T40 layer and a very sharp transition once the dielectric is fully recessed, which is the case at approximately 57 s in Fig. 8(b). Using this method, precise etching can be achieved with reliable automated endpoint detection system.

After recessing the dielectrics, stress was measured again to monitor the stress relaxation effect through partial removal of the dielectric material. Fig. 9 shows stress relaxation on AlGaN/GaN-on-Si wafers after recessing 2NN multi-layers of 200 nm (Fig. 9(a) and (c)) and 1.5 µm (Fig. 9(b) and (d)) thickness. Both examples show almost no change in bow and the absolut change in stress is less than 30 MPa of compressive stress for thick and thin dielectric. The visible surface roughness on all wafer surfaces comes from pre-processed metal and via structures.

The resulting via shape (Fig. 9(e)) allows for good metallization with sputter deposition. The individual layers show slightly different angles and lateral etch rates, with an opening angle at the via top side. Example interconnection in a via chain is shown in Fig. 9(f).

4. Electrical characterization

For dielectric breakdown qualification, current (I)-voltage (V) measurements on MIM capacitors up to 2 kV were done using a Keithley 4200A-SCS Source Measure Unit (SMU) on a semi-automatic MPI TS2000-HP wafer probe station at 23 locations on the wafer. E_{bs} and leakage currents (I_L) were extracted. All breakdown measurements were executed using 3M Fluorinert FC-40 high insulating fluid previously applied to the surface.

The MIM capacitors were produced with the respective PECVD dielectric as insulator on w-SiO_2/Si wafers. After forming the lower metal pads by Ti/AlSiCu (20/1000 nm) sputter deposition and Inductively Coupled Plasma (ICP) RIE etching, the metal was annealed at 400

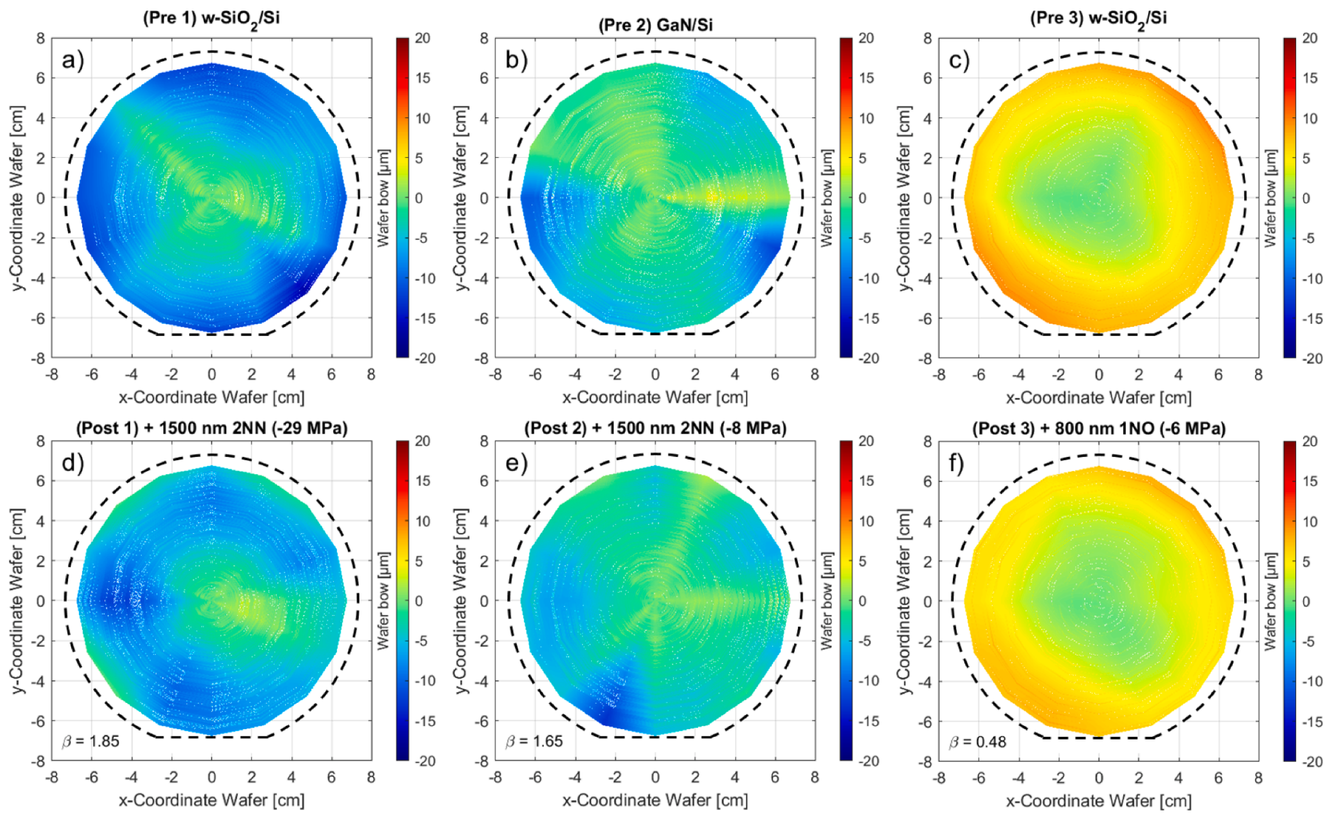

Fig. 7. Measured wafer bow of 150 mm w-SiO$_2$/Si and AIXTRON SE AlGaN/GaN-on-Si wafers before (a)–(c) and after (d)–(f) 2NN and 1NO PECVD deposition. The resulting bow was optimized and stresses were kept minimal within the stacks deposited, no visible change in wafer bow is present despite the high dielectric thickness. The visible surface roughness comes from the metal structures on the wafers.

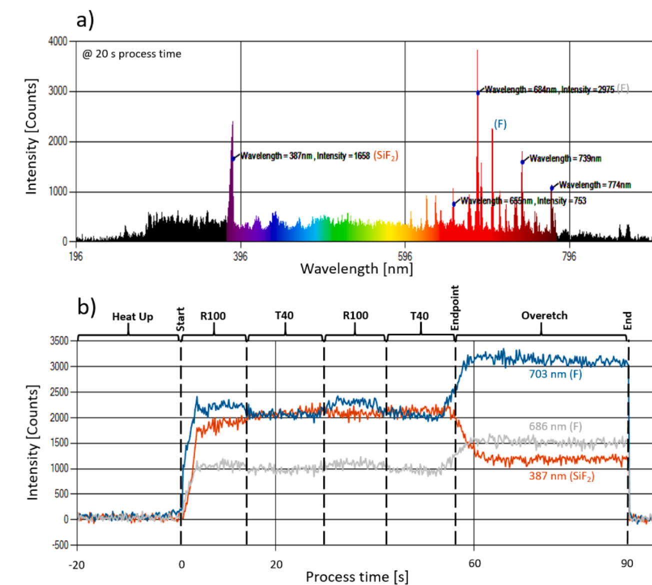

Fig. 8. Measured etching spectrum(a) of SF$_{6/Ar}$-based RIE of 2NN and time plot (b) of the characteristic lines at 703 nm (F), 686 nm (F) and 387 nm (SiF$_2$). The endpoint of the process is clearly visible around 57 s. T40 and R100 both show different spectroscopic intensities during etching, which is especially visible in the 703 nm line.

°C for 5 min. In the following, PECVD deposition of the single layers or multi-layers was done. The PECVD dielectric was opened in the pad region with a SF$_6$/Ar-based RIE process. The top metal pads of the capacitors were done by another Ti/AlSiCu (20/1000 nm) sputter deposition with consecutive ICP RIE structuring.

The single films as well as the multi-layers were investigated as dielectric materials. The MIM capacitors were stressed with linearly increasing V while I_L was monitored until soft and hard breakdown occured. However, the relevant dielectric characteristic in this work is not hard breakdown, but soft breakdown criteria. Soft breakdown of the single and multi-layer dielectrics was defined at the point, where $I_L = 1$ nA/mm^2. The measured MIM area was 0.25 mm^2 for single layers and 0.49 mm^2 for multi-layer dielectrics. Fig. 10 shows the individual mesurements and histograms of soft breakdown events of single films and multi-layers with different thicknesses. The histogram is fitted with the corresponding Weibull distribution of the soft breakdown events.

The single films show soft breakdown values of 0.56 MV/cm for O40, 2.82 MV/cm for T40 and 2.32 MV/cm for R100. I_L is consistently inreasing with applied stress voltage until hard breakdown occurs. The SiN$_x$ films T40 and R100 are relatively similar in terms of soft breakdown and leakage behaviour despite the opposite stress values and the different deposition recipes. In contrast to this, O40 has a much smaller soft breakdown point which is around five times smaller than that of the SiN$_x$ films. All layers show a increase of current before breakdown, which can be explained by the formation of a percolation path within the dielectric. This continous increase of I_L is also seen in the multi-layers. However, the current of the multi-layers is noisy before breakdown and shows higher jitter, while the current of the single films show a smooth increase. This difference can be explaind by the way of formation of the leakage or percolation path. While a single film shows a continuous formation, which is shown in the $I - V$ curve by a smooth increase of leakage current, the SiN$_x$/SiN$_x$ multi-layers in contrast develop the path in a more abrupt way with simultaneous change in the electric field distribution due to the presence of interfaces. The 1NO multi-layer do not show the same noise in the leakage current in the region below soft breakdown, but increased noise after the soft

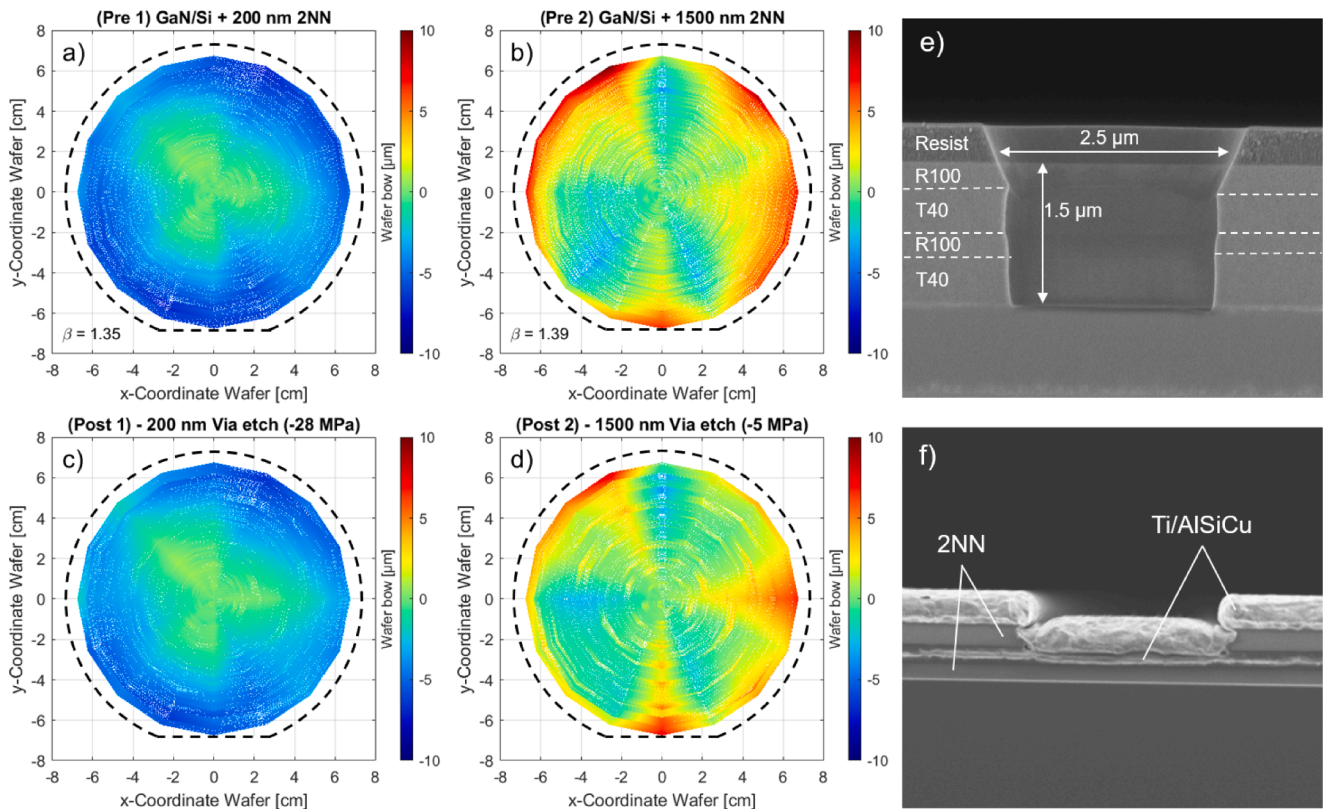

Fig. 9. Measured wafer bow of 150 mm AIXTRON SE AlGaN/GaN-on-Si wafers with 200 nm and 1500 nm 2NN before (a), (b) and after (c), (d) SF_6/Ar-based RIE with 50% mask opening. Removing part of the passivation leads to partial stress relaxation below − 28 MPa. The visible surface roughness comes from the metal structures on the wafers. (e) shows a typical via shape after RIE with characteristic edges depending on the material within the stack and (f) shows a larger via after sputter metallization.

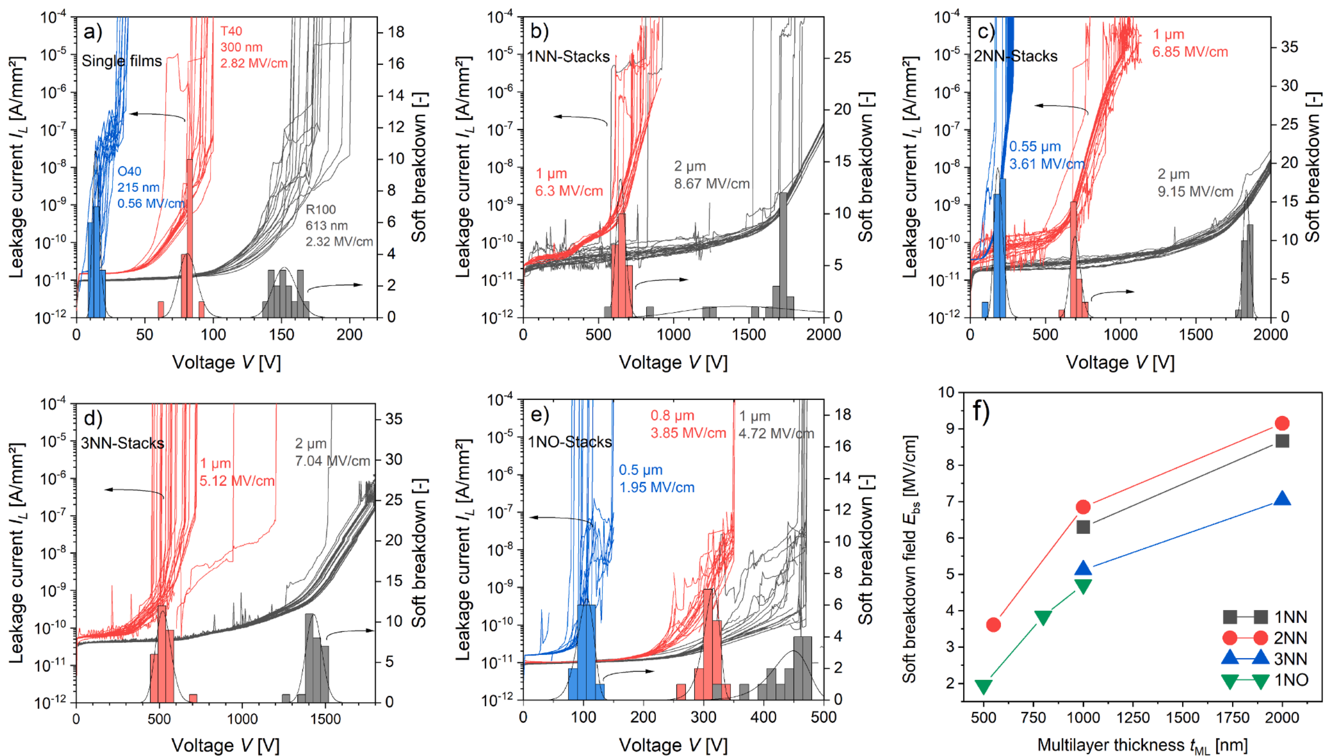

Fig. 10. Measured dielectric soft breakdown behaviour and histogram statistics of MIM capacitors with single films (a), 1NN (b), 2NN (c), 3NN (d), 1NO (e) multilayer dielectrics and summary (f) at different thicknesses.

breakdown criteria is passed.

The 1NN, 2NN and 3NN multi-layers all show identical behaviour and comparable leakage currents as well as jitter. However, there is a difference in soft breakdown strength with the total number of layers included in the multi-layer as well as with total stack thickness. All multi-layers reach higher soft breakdown strengths as the total thickness increases, where small thicknesses of multi-layers (< 600 μm) have higher E_{bs} compared to the single films. The 550 nm thick 2NN (Fig. 10 (c)) is the most comparable example and reaches 3.61 MV/cm, which is above the soft breakdown of the single T40 and R100 layers. When the multi-layer thickness is increased, E_{bs} also reaches higher values. There is a thickess-independent trend with the number of layers in the multi-layer, where 2NN reaches highest soft breakdown strength with 6.85 MV/cm at 1 μm and 9.15 MV/cm at 2 μm total thickness and 3NN reaches lowest. The 2 μm thick 2NN does not reach hard breakdown in the measurement up to stress voltages as high as 2 kV. Although 1 μm thick 2NN reaches higher values of soft breakdown srength compared to the 1NN and 3NN counterpart, the leakage current is sligthly higher in the sub-breakdown region and shows a broad distribution and high noise. This might be related to process fluctuations during multi-layer deposition. A comparative plot of the soft breakdown strengths with thickness is given in Fig. 10(f). The 2NN multi-layer shows a nonlinear increase of E_{bs} with thickness between 550 nm and 2 μm. All SiN_x/SiN_x multi-layers show a consistent increase between 1 μm and 2 μm. However, it can clearly be seen that the 2NN shows the highest breakdown strengths at small leakage currents over a thickness range of 550 nm up to 2 μm. The 1NO multi-layer shows the smallest soft breakdown strengths of the multi-layers with 1.95 MV/cm at 500 nm, 3.85 MV/cm at 800 nm and 4.72 MV/cm at 1 μm thickness. The high soft breakdown strength of 2NN is probably a result of optimum interfaces, distances and field distributions that prevent charge propagation and therefore leakage path formation across multi-layer films, which increases the dielectric strength (Gefle et al., 1997; Hanby et al., 2019).

Multi-layered dielectrics in MIM configuration are influenced by interface polarization effects like the Maxwell–Wagner effect (Jinesh, Lamy, Klootwijk, & Besling, 2009). This effect of enhanced charge migration to dielectric interfaces is present when the conductance difference between the individual layers of the multi-layer is high. High conductance differences lead to asymmetrick leakage and different relaxation times depending on the carrier injection direction in the MIM structure. $I-V$ measurement of the same MIM structures with 2NN dielectric (Fig. 11) was done with carrier injection from the high pad (R100 side) and from the low pad (T40 side). While the high pad measurement correspond to the results from Fig. 10, the low pad measurement shows slightly different breakdown strength of 6.5 MV/cm with less carrier injection. Despite the fact that breakdown strength is different, the carrier injection difference is small and not present below 300 V.

Measurement of 2NN dielectric constant (ϵ_r) at 550 nm thickness as shown in the wafer map of Fig. 12, shows high uniformity over the substrate area and a mean value of 7.15 at 25 °C. The 2NN multi-layer ϵ_r therefore is comparable to single layer SiN_x (Lenka & Panda, 2012).

In order to extract the statistical soft breakdown behaviour of the MIM capacitors, Weibull analysis was done. Aim of the analysis was to extract the shape parameter or Weibull slope (k) of the dielectrics which characterizes the probability distribution with stress voltage. High values of k mark a sharp transition between the safe-operation and failure region, which means that the probability of failure rapidly rises once a certain stress voltage is surpassed. Small k-values on the opposite describe a slow increase of failure probability with stress voltage and therefore a much wider range of voltages where devices might fail due to soft breakdown event. Generally a sharp transition with high k-values is desired in order to operate a dielectric close to its limits but without high failure probability. Weibull statistics for soft dielectric breakdown were extracted and plotted in Fig. 13. The Weibull distribution over E_{bs} ($P(E_{bs})$) is defined as Andersen & Dennison (2015); Chauvet & Laurent (1993)

$$P(E_{bs}) = 1 - e^{-\left(\frac{E_{bs}}{E_0}\right)^k}, \quad (18)$$

where E_0 is the electric field with a breakdown probability of 63.2%. The 1NN, 2NN and 3NN multi-layers show higher k in the range of 9.7 to 91.6 compared to 1NO with values between 8.8 and 20.1. The values of k are directly related to the propability of soft breakdown within a certain range of applied electric fields and translates to the slope of the fitted linear curve in the logarithmic plot. The highest k was achieved for 2 μm 2NN with 91.6. The multi-layer behaviour is similar to the single layer behaviour, where O40 also has a smaller k of 6.6 compared to 17 of T40 and 19.5 of R100.

5. AlGaN/GaN-on-Si HEMT characterization

After investigation and characterization of different multi-layer dielectrics, the 2NN was adapted within CMOS-compatible HEMT processing at IMS CHIPS (Moser et al., 2022; Pradhan et al., 2021; Pradhan et al., 2022) on 150 mm AlGaN/GaN-on-Si wafers. The manufactured devices are designed for power applications with high-level interconnections, where a sufficient voltage shielding is necessary. An overview of the schematic process flow as well as device design and

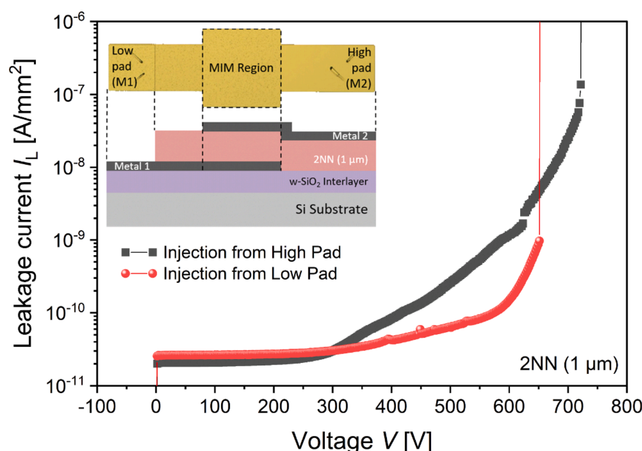

Fig. 11. Maxwell–Wagner instability measurements by charge injection from high and low pad of the MIM capacitor.

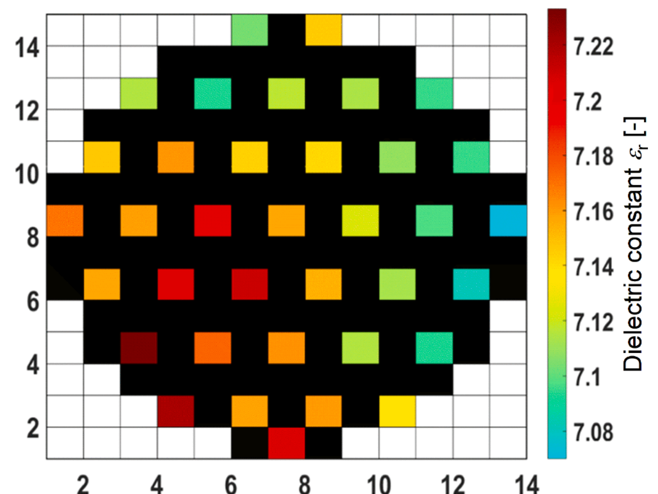

Fig. 12. Wafer map of dielectric constant extracted from 550 nm thick 2NN multi-layer.

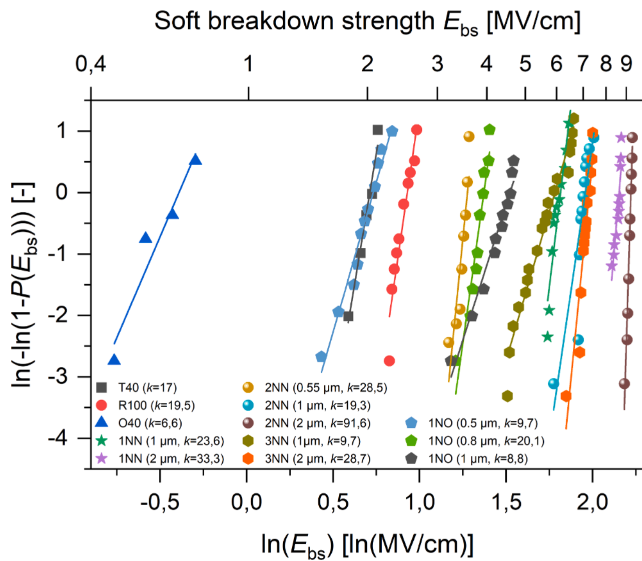

Fig. 13. Soft dielectric breakdown Weibull diagram of single and multi-layer dielectrics.

dimensions is given in Fig. 14. Although multi-finger devices were processed, the characterization was conducted on small PCM structures, in order to better observe the small nA leakage of the SiN_x layers, without influence of other parasitic leakages in large devices. Within this work three device designs were investigated: Metal-Insulator-Semiconductor (MIS) HEMTs with Source Field Plate (SFP) and Schottky-HEMTs with and without SFP. All devices have a width of 100 µm and a gate length of 1 µm and are designed with two source-fingers, although only a single finger was measured. Measurements were executed on a Keithley 4200A-SCS SMU.

Processing starts with Metal-Organic Chemical Vapour Deposition (MOCVD) epitaxy of GaN epi-layer stack on 1000 µm thick $p\text{-}Si_{(111)}$ substrates in an AIX G5+ C2C Planetary MOCVD reactor at AIXTRON SE (Heuken et al., 2019). A 200 nm mesa isolation is recessed, followed by surface passivation using 130 nm LPCVD Si_3N_4 at IMS CHIPS. Drain, source and gate contacts are opened by recessing the Si_3N_4 and 10 nm LPCVD Si_3N_4 gate dielectric is deposited. After removal of the gate dielectric from the ohmic and Schottky regions, Atomic Layer Etching (ALE) is used to recess the AlGaN barrier, followed by evaporation and structuring of Ti/Al (10/200 nm) contacts using lift-off technique. Ohmic contacts are formed by annealing in N_2 ambient at 450 °C for 10 min. Ni/Ti/Al (50/10/200 nm) gate contacts are evaporated and structured with lift-off as well. Since the gate dielectric was intentionally removed by mask design from some devices, both Schottky and MIS devices are present. After formation of core contacts, the first PECVD 2NN multi-layer dielectric is deposited with a thickness of 200 nm functioning as SFP dielectric. This 2NN SFP dielectric is used to reduce the electric field spikes at the drain-edge of the gate electrode (Adak et al., 2014; Liu & Kang, 2011). The voltages between the source and gate usually are within the range of $+2 \leq V_{gs} \leq -12$ V, which translates to a maximum electric field strength of 0.6 MV/cm. In the contact areas, via openings are recessed by SF_6/Ar RIE and Ti/AlSiCu (20/1000 nm) SFP metal is sputter deposited and structured by Cl_2/BCl_3/HBr RIE ICP. The second dielectric is used to shield the electric field between the high-level metal interconnects of interdigitated comb structures and the SFP metal, where a maximum voltage of 650 V is present. A 1.5 µm thick 2NN multi-layer dielectric is deposited, which gives a electric field of 4.3 MV/cm, which easily can be shielded by the 2NN according to Fig. 11. After another via opening etch, the Metal 1 metallization (Met1) is done by Ti/AlSiCu (20/2000 nm) sputtering and back etching.

During HEMT production the wafer bow was continuously monitored as shown in Fig. 15 along with the associated schematic device cross-section at each step. The wafer bow after MOCVD epitaxy is within ±10 µm, which is comparable to current state-of-the-art GaN-on-Si epitaxy substrates (Cheng et al., 2006; Cordier et al., 2009; Heuken et al., 2019; Marcon, Saripalli, & Decoutere, 2015). Processing until formation of gate contacts is summarized in Fig. 15 under “Core HEMT” and usually induces only little to no stress to the wafer. Deposition and etching of 200 nm SFP dielectric also does not lead to high changes in wafer bow. Once the 1 µm thick SFP metal is introduced, the bow changes from convex to concave shape due to the high thermal mismatch between the dielectric and the metal. Structuring of the SFP partially relaxes the substrate, although the bow remains concave. The

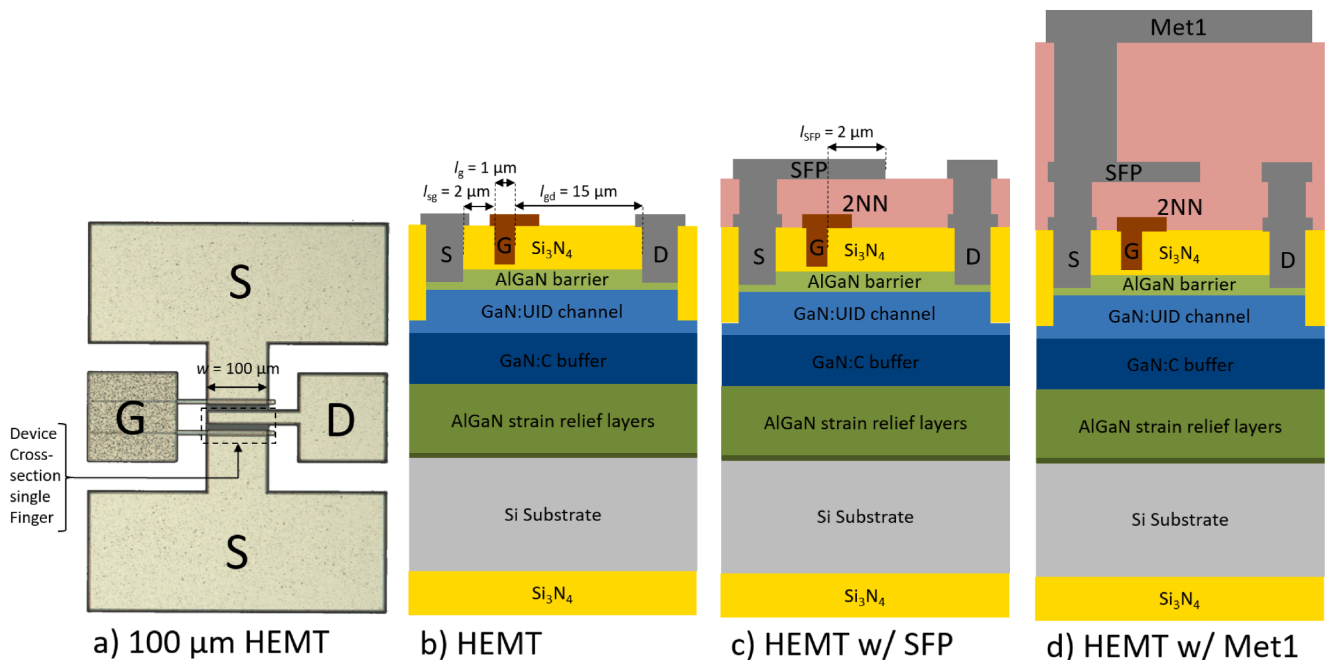

Fig. 14. Overview of test devices: Two-Finger-HEMT top-view with a width of 100 µm (a) and device cross-sections of a single finger at the MIS-HEMT (b), SFP (c) and Met1 stage (d).

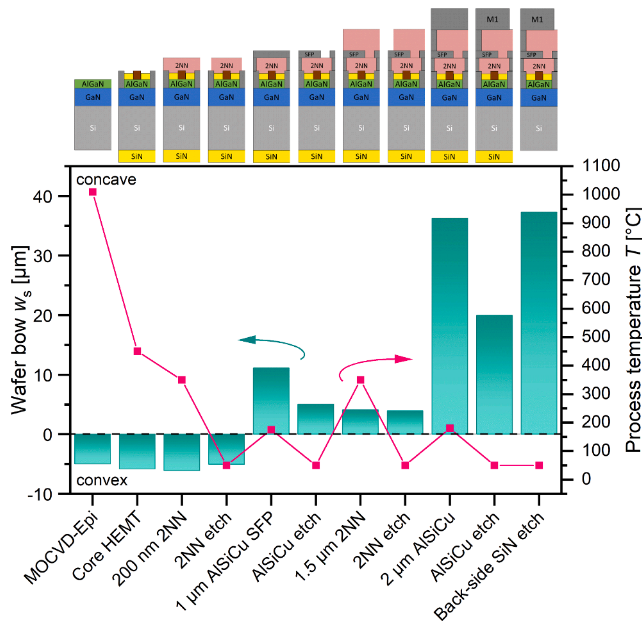

Fig. 15. Measured wafer bow of 150 mm AIXTRON SE AlGaN/GaN-on-Si wafer at different process steps of HEMT device manufacturing. Due to stress-balanced 2NN PECVD multi-layer deposition, the wafer bow is kept small in order to ensure an even surface for processing and machine handling.

following 1.5 µm thick 2NN power dielectric was designed with $\beta = 1.5$ and reduces the wafer bow to 4.8 µm. The last steps of device production include 2 µm metal interconnect deposition and structuring as well as back-side LPCVD Si_3N_4 removal. These steps introduce higher stress to the substrate and increase the bow at the end of the process to 36.3 µm. However, the wafer bow is always kept within the limitations of ±50 µm even though the temperatures range from room temperature to 1000 °C and several thick dielectrics and metals are deposited.

Device output and transfer characteristics of the MIS-HEMT is shown in Figs. 16 and 17(a) at different production stages. The additional passivation and metallization layers lead to a current increase with each additional stage by adding SFPs and increasing the metal thickness. In general, overall device characteristics were enhanced by adding SFP and Met1 stage using PECVD 2NN dielectric.

Off-state leakage measurements of drain (I_{ds}) and gate (I_{gs}) current in the MIS-HEMT at $V_{gs} = -9$ V show scaling behaviour with the three production stages (Fig. 17(b)). Drain leakage at the HEMT stage is 34 nA/mm at $V_{ds} = 5$ V and decreases once the SFP is introduced to 0.3 nA/mm. After structuring of Met1, off-state drain leakage slightly increases again to 1.4 nA/mm. Gate leakage continously decreases as higher levels of metallization are added. While at HEMT stage 2.1 nA/mm were measured at $V_{ds} = 5$ V, leakage decreases to 0.4 nA/mm after SFP structuring and to 0.2 nA/mm after Met1. Leakage currents at Met1 stage (Fig. 14(d)) are constant up to a bias of 200 V and do not show sudden increase or breakdown as can be seen in the off-state stress measurement from Fig. 17(c). The measurement bias here is limited by the device design (l_{gd}).

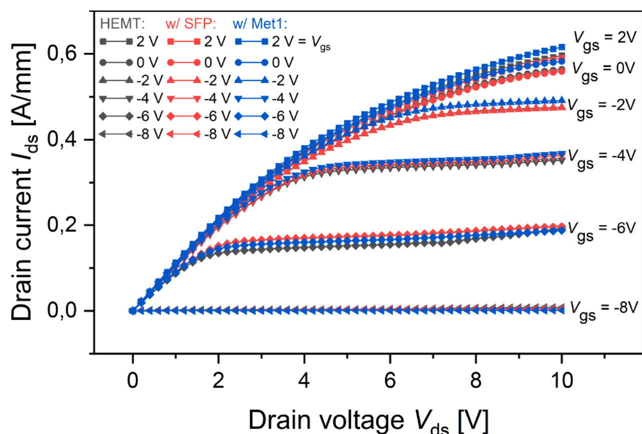

Fig. 16. Output curves of a MIS-HEMT at different process stages showing the influence of additional passivation and metallization.

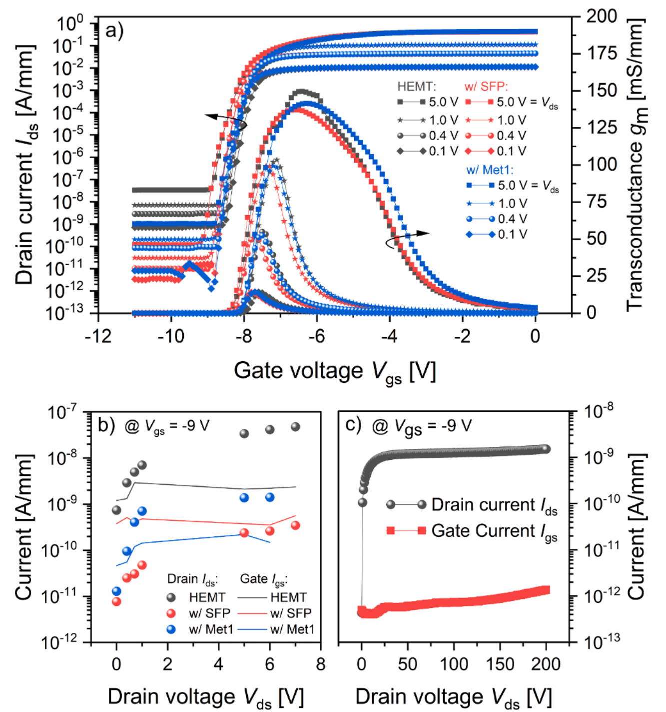

Fig. 17. Transfer curves (a) and off-state leakage (b) of a MIS-HEMT at different process stages. (c) shows leakage at Met1 stage up to 200 V.

Dynamic measurements with a pulse width to period width ratio of 1 µs/100 µs were executed to characterize drain and gate lag (Fig. 18). The measurements points were extracted at $V_{gs} = 0$ V for both measurement series. The measured devices were Schottky-HEMTs with and without SFP and a MIS-HEMT with SFP at Met1 stage to allow for comparison between different configurations. Drain lag (Fig. 18(a) is within the same order of magnitude for all three variations. At measurement point $V_d = 20$ V, the Schottky-HEMT without SFP has only 98.1%, the Schottky-HEMT with SFP has 94.6% and the MIS-HEMT with SFP 94.9% current reduction. At $V_d = 40$ V, the Schottky-HEMT without SFP is further reduced to 88.2%, the Schottky-HEMT with SFP reaches 83.5% and the MIS-HEMT with SFP 89% of the maximum current. Pulsing the gate to provoke gate lag (Fig. 18(b)) at −1 V, −2 V, −2.5 V and −3 V for Schottky devices and −9 V, −10 V, −12 V and −15 V for the MIS device proved no remarkable gate lag effect in the DuTs. The Schottky device without SFP shows the highest current reduction to 97.2% $I_{d,max}$ at −3 V. The 2NN passivated devices therefore show negligible gate lag and comparatively small drain lag at Met1 stage.

6. Conclusion

Within this study we developed and investigated PECVD SiN_x and SiO_y single films as well as SiN_x/SiN_x and SiN_x/SiO_y dielectric multi-layers for high voltage applications for a wide voltage range up to 2 kV. Apart from the electrical and device properties, the study focuses on the mechanical properties of the deposited layers and the multi-layers were designed in a stress-compensated way, which does not change

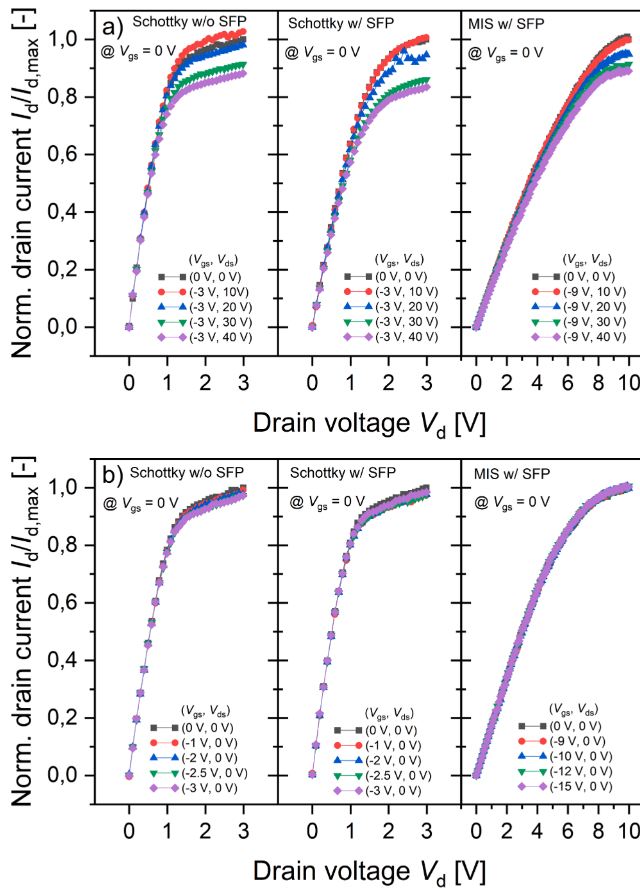

Fig. 18. Drain lag (a) and gate lag (b) measurements on Schottky devices with and without SFP and a MIS device with SFP.

wafer bow for deposited thicknesses as high as 2 µm. Through simulation of multi-layer stresses with the layer thickness ratio, active wafer bow correction is possible, too.

Mechanical properties were first investigated on w-SiO_2/Si wafers by monitoring wafer bow changes before and after deposition or etching steps. The developed SiN_x films show opposite stress values of 436.82 MPa for T40 and − 942.84 MPa for R100, while O40-SiO_y has − 243 MPa with high long-term stability. The opposite stress values allowed for the formation of layer stacks with alternating layers of T40/R100 and T40/O40 which are designed in a way that the total stress is compensated or managed to correct an already present wafer bow. The stress-neutral point for 1NN, 2NN and 3NN multi-layers was found to be at $\beta = 1.75$, while 1NO was stress-neutral at $\beta = 0.45$. For thickness ratios above or below the stress-neutral point for each stack, resulting stress scales non-linear.

The soft dielectric breakdown field strength was investigated using MIM capacitors. The individual layers were developed with E_{bs} of 2.82 MV/cm for T40, 2.32 MV/cm for R100 and 0.56 MV/cm for O40. multi-layers proved to be more efficient at blocking high voltages at the same thicknesses compared to the single films. Best results were achieved with the 2NN configuration with 6.85 MV/cm and 9.15 MV/cm for total thicknesses of 1 µm and 2 µm, respectively.

Deposition of 2NN on GaN-on-Si substrates proved the transferability to other substrate types and allowed processing of GaN HEMT devices. The GaN HEMT process was executed with the beforehand developed 2NN dielectric as insulation for high-level metal interconnects and SFPs. The processed wafers show a small bow within ±50 µm over the full production and exhibit good HEMT device behaviour throughout different processing steps as well as small off-state leakage.

CRediT authorship contribution statement

Matthias Moser: Investigation, Methodology, Visualization, Writing – original draft. **Mamta Pradhan:** Formal analysis, Software, Writing – review & editing. **Mohammed Alomari:** Conceptualization, Supervision, Writing – review & editing. **Michael Heuken:** Resources, Writing – review & editing. **Thomas Schmitt:** Resources, Writing – review & editing. **Ingmar Kallfass:** Writing – review & editing. **Joachim N. Burghartz:** Writing – review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data Availability

The data that has been used is confidential.

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