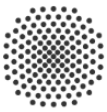

Universität Stuttgart
Institut für Nano- und Mikroelektronische Systeme

Measurement Setup Design for a wide dynamic range photodiode readout ASIC

Research Project

at the Institute for Nano- and Microelectronic Systems of the University of Stuttgart in cooperation with the Institute for Microelectronics Stuttgart

By

Kiran Mulik

28. April 2023

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Examiner	Prof. Dr. Jens Anders
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Affidavit

I hereby declare that I have independently written the present thesis and have not used sources or aids other than those indicated. All statements taken verbatim or paraphrased from external sources are marked accordingly. The thesis has not been submitted in the same or a similar form as part of any other examination or study. The electronic version of this thesis submitted is identical to the bound copies.

Stuttgart, 28. April 2023

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(Kiran Mulik)

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1 Introduction to Ge-on-Si Detectors

Near-infrared (NIR) detectors are specialized sensors that detect and quantify light in the near-infrared spectrum. These detectors have diverse applications, including medical imaging, remote sensing, and industrial monitoring[1]. NIR detectors based on silicon have undergone significant development and are considered highly advanced, especially in the case of germanim on silicon(Ge-on-Si) structures. Ge is well-suited for absorption above 1.1 μm and is highly compatible with silicon technology, which remains the dominant and most effective technology for these detectors.[2,6]

Indium gallium arsenide (InGaAs)-based NIR detectors have long been the preferred choice for high-performance NIR detection due to their exceptional sensitivity in the NIR range. However, their high production costs have hindered widespread adoption. InGaAs detectors necessitate complicated fabrication procedures that entail epitaxial growth on a semi-insulating substrate, rendering them incompatible with standard complementary metal-oxide-semiconductor (CMOS) technology[2,3].

Ge-on-Si detectors provide an alternative to InGaAs detectors, using germanium (Ge) as the absorbing material and silicon (Si) as the substrate. Ge possesses a high absorption coefficient in the near-infrared range, making it a suitable material for NIR detection [4,9]. However, Ge and Si have different lattice constants which leads to one of its main problems, the mismatch between their lattices which can create defects and reduce detector efficiency. Along with that, dark current is also a critical factor that affects the sensitivity of these detectors. The dark current observed in Ge pin photodiodes (PDs) on Si is more than one order of magnitude higher compared to that observed in InGaAs PDs[5,13]. It is an open challenge now to find ways to minimize the impact of dark currents on NIR detectors to achieve high sensitivity for the detection of weak optical signals.

Despite these limitations, Ge-on-Si detectors offer several advantages over other NIR detectors, including the ability to integrate with standard Si electronics, resulting in lower costs and compact and portable device development [10].

NIR Ge-on-Si detector cameras use CMOS technology for their readout circuits, which involve various components such as transistors to convert analog signals into digital signals for processing and storage. The readout circuit consists of an array of CMOS transistors that act as both amplifiers and switches. The amplifiers boost the analog signals produced by the detector, while the switches determine which signals are selected for processing. The capacitors then store the amplified signals, which are subsequently converted into digital signals through an analog-to-digital converter (ADC).

However, as mentioned above, the readout circuit's sensitivity is limited by the amount of dark current generated, which can affect the detector's performance and increase noise levels. To minimize the impact of dark current, the p-i-n photodetectors are optimally operated at zero bias[8], which will be described in detail in this thesis. This approach helps to achieve high sensitivity and low noise levels in NIR Ge-on-Si detector cameras.

The background of the thesis is to develop NIR cameras/spectrometers based on Ge-on-Si technology. Figure 1 demonstrates the setup of the spectrometer developed in the NASIKA joint project. The camera system as well as the spectrometer comprises a photonics chip with a sensor array, an an application-specific integrated circuit (ASIC) for readout, a microcontroller with a 12-bit ADC, and a universal serial bus (USB) interface to a graphical user interface on a computer. This research project examines the readout integrated circuit of the NASIKA photonic chip.

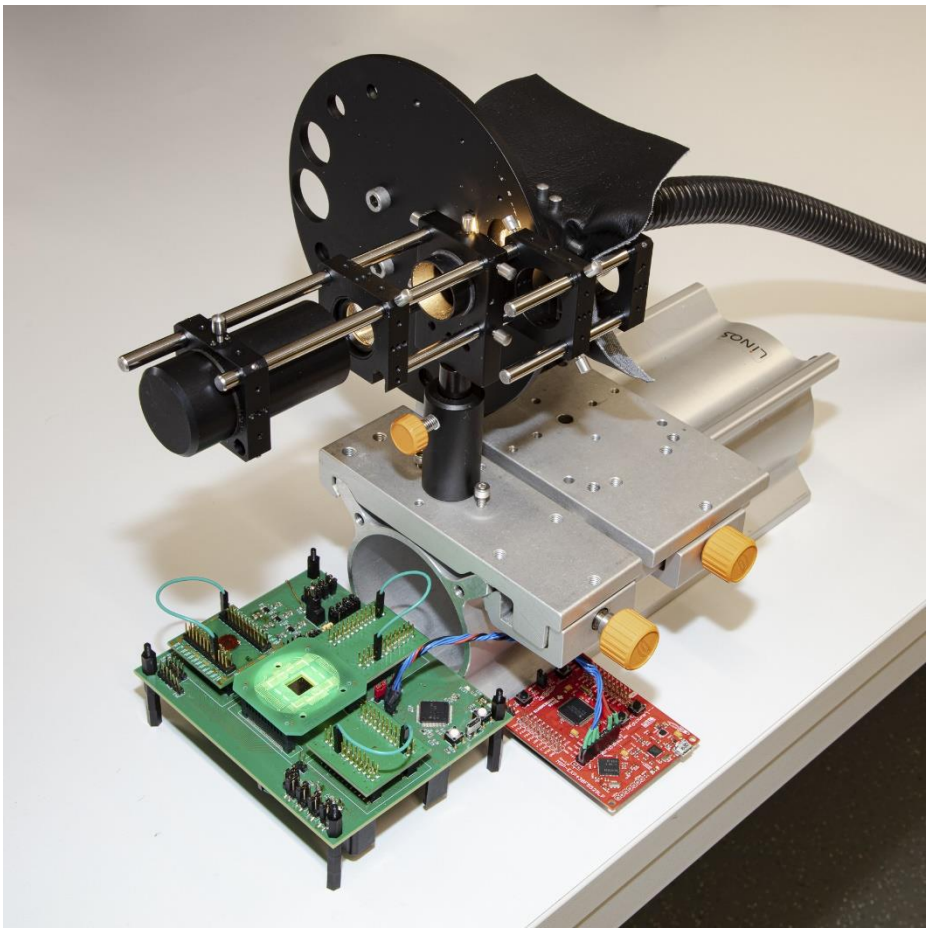

Figure 1 Measurement Setup of the Spectrometer- NASIKA

2 Introduction to Project Goal

The goal of this thesis is to study the peripheral readout circuitry used with the aforementioned Ge-on-Si detector. The architecture of the ASIC is presented, with a functional illustration for every block. The two methods of readout for two versions of the ASIC are described and analyzed in the thesis. The simulation results of the pixel readout speed and the dynamic range are presented. Finally, the measurement setup is described & compared with the simulation results.

This thesis focuses on the ASIC simulations, generation of test clock patterns using Cadence Virtuoso & MSP430F5529 microcontroller. In this chapter, the peripheral circuit design of the analog front-end readout circuit is described, as well as point of differences of the two versions of the ASIC described later. Chapter 3 illustrates the PCB Design for the photonic chip followed by a description and analysis of the simulation test bench on Cadence Virtuoso. The thesis concludes with the overview of the programming used in the microcontroller.

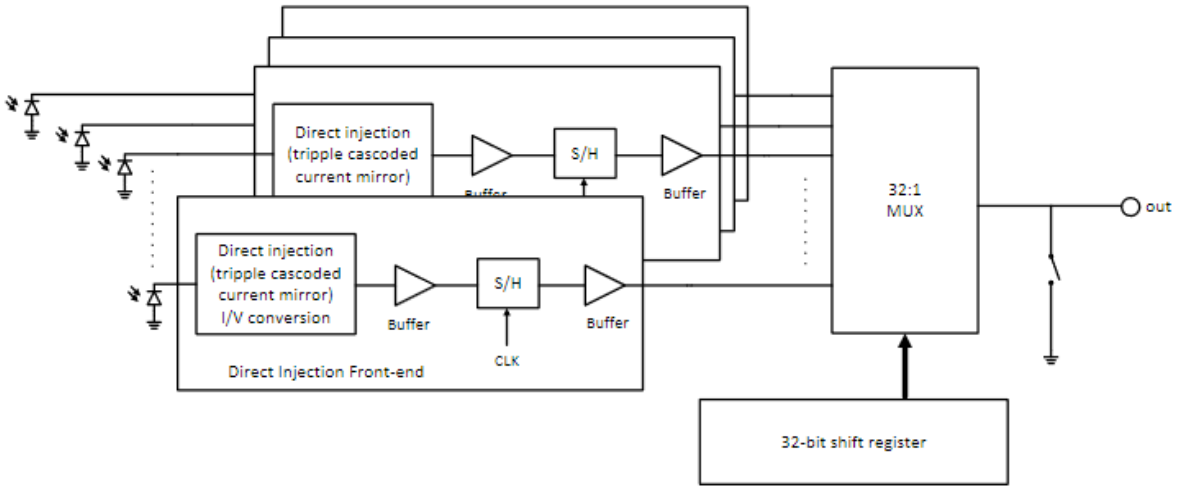

Figure 2: ASIC Block Diagram

2.1 ASIC Characterization

The ASIC is a crucial component of the Ge-on-Si photonic detectors. This chapter will focus on the characterization of the ASIC used in the readout of the photonic chip. The photonic detectors are composed of a thin layer of Ge deposited on a Si substrate. The Ge layer absorbs photons in the NIR region and generates an electrical signal, which is then detected and processed by the associated readout integrated circuit i.e. the ASIC. To achieve optimal performance from the detectors, it is essential to carefully control the operating conditions,

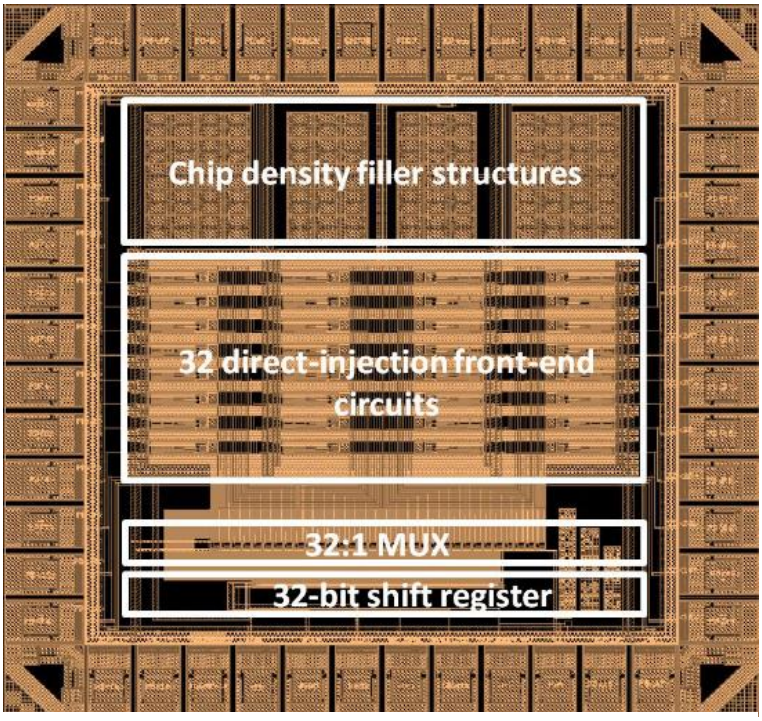

Figure 3: ASIC Layout

including bias voltage and temperature. It has been established that operating the detectors under a near-zero bias voltage improved their sensitivity and reduced the dark current. The reduced dark current is critical because it minimizes the noise floor of the detectors and improves their signal-to-noise ratio (SNR), allowing for the detection of weaker signals.

The ASIC used in the readout of the photonic chip is specifically designed for this purpose and consists of 32 direct injection front-end circuits, a 32:1 multiplexer, and an output reset switch. The ASIC is implemented in the XFAB XH018 0.18μm CMOS technology, which is known for its high performance, low power, and small-area features.

The direct injection front-end circuits(Figure 4) are responsible for receiving and processing the photocurrent generated by the photodiodes. To achieve a zero-volt biasing of the photodiode and a low input impedance, the photocurrent is injected into the ASIC via a current injection unit.

After the photocurrent is injected into the readout branch, a current-to-voltage conversion is applied to convert the current into a voltage signal, which is then buffered and sampled. The sampling actions for all 32 channels happen simultaneously, which is referred to as a global shutter function. This ensures that all channels are sampled at the same time. The sampled voltages are then buffered again and read out in a time-multiplexed way by the 32:1 multiplexer. During the inactive phase of the multiplexer, the output is tied to the ground via the reset switch. This prevents any residual charge from affecting subsequent readings and ensures a clean output signal.

The ASIC layout is shown in Figure 3 and has a chip area of 1.5 mm × 1.5 mm, making it a compact and highly integrated solution for the readout of the photonic chip. The supply voltage for the ASIC is 3.3 V. Each block of the readout chip is described below.

2.1.1 Current Mirror

A current mirror circuit is a common circuit used in electronics to replicate or mirror a current through a second circuit. In this implementation, the current mirror circuit is used to inject the photocurrent from the Ge-on-Si detectors into the readout circuitry. The circuit is designed with triple cascoded PMOS and NMOS transistors to ensure that identical currents flow through both the left and right branches of the circuit. When a current flows through

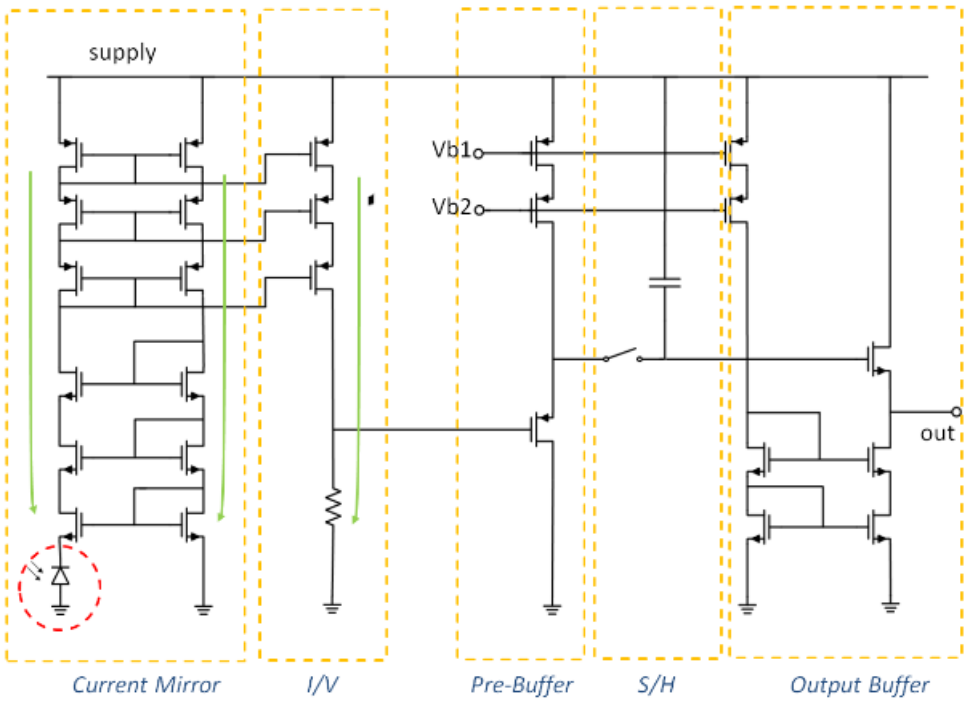

Figure 4: Direct Injection Front-End Circuit

the left branch of the current mirror, it is copied to the right branch via the upper PMOS

current mirror. Then, the current is copied back to the left branch again via the bottom NMOS current mirror. The currents flowing in the left and right branches are identical, which forces the gate-source voltages of the bottom two N-type MOSFETs (M1 and M2 in Figure 5) to be identical as well. This creates a near 0 V biasing across the photodiode.

The benefit of this near 0 V biasing is that it minimizes the leakage current flowing in the shunt-resistance of the photodiode which instead is injected into the current mirror circuit. Shunt resistance is a parasitic resistance between the cathode and anode of the photodiode when no light is present. It can negatively impact the photodiode's performance by contributing to dark current and reducing the signal-to-noise ratio. Dark current refers to the current that flows through a photodiode in the absence of light and can increase noise hence limiting the sensitivity and accuracy of the photodiode.

However, by biasing the photodiode at or near 0V, the dark current is greatly reduced, leading to a higher signal-to-noise ratio and improved accuracy of measurements.

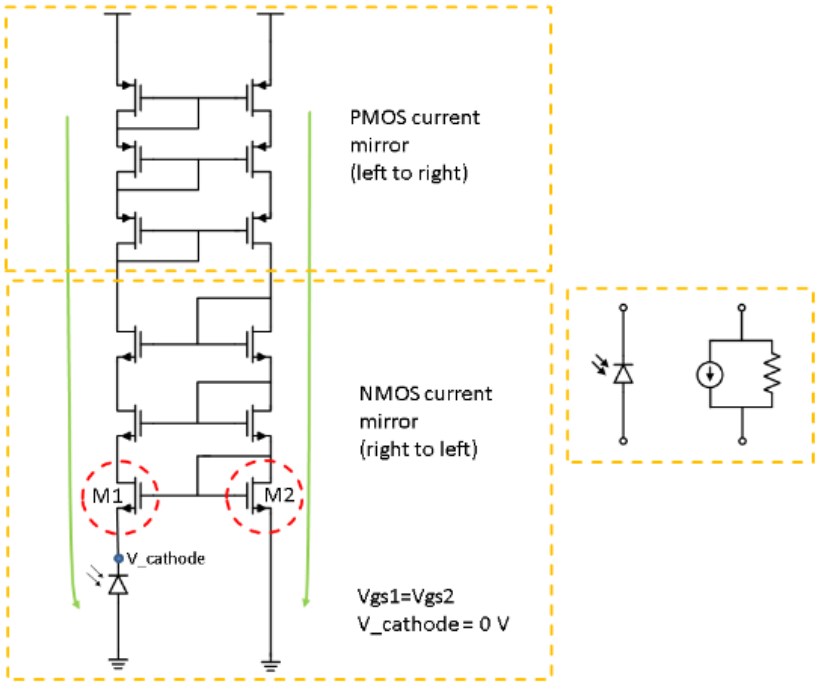

Figure 5: Triple Cascoded Current Mirror

2.1.2 I/V conversion

The photocurrent produced by the Ge-on-Si detectors is an important signal that needs to be converted into a voltage signal for further processing by the ASIC. The detailed description of this stage is given further in this chapter when two versions of the ASIC are described.

2.1.3 Pre Buffer/ Output Buffer

A pre-buffer is used after the I/V conversion stage. This is necessary because the I/V conversion is done via a resistor/capacitor, which introduces a high-impedance node in the circuit. Without the pre-buffer, the voltage at this node could be affected by external noise, which would negatively impact the signal-to-noise ratio (SNR) of the photonic chip.

The pre-buffer used in this design is a PMOS source follower, which has a gain slightly lower than unity. The buffer's role is to provide a low-impedance output, ensuring that the voltage at the I/V conversion node is not disturbed by external noise. The pre-buffer is connected to a sample-and-hold (S/H) stage(Figure 4), which is controlled by the global-shutter clock (CLK) signal. A minimum CMOS switch for lowest charge-injection and clock feedthrough error is used for the S/H stage. Charge injection can cause errors in the output voltage of the circuit and degrade the performance of the circuit. The use of a minimum CMOS switch helps to minimize the amount of charge injection that occurs when the switch is turned ON. The S/H stage allows the voltage level at the I/V conversion node to be sampled and held during the readout process, ensuring that the output is stable and accurate.

The output of the pre-buffer is then connected to an NMOS source follower, which provides additional buffering and low-impedance drive capability. The PMOS and NMOS source follower buffers used in the photonic chip need to be biased properly to function correctly. This biasing current is generated by a current generation circuit that uses two diodes, Vb1 and Vb2(Figure 6), to generate a voltage that is then fed to each channel. The external resistor, which is set at a default value of 400 kOhm, is used to create a biasing current of around 2 μA, which is then mirrored into the core circuit.

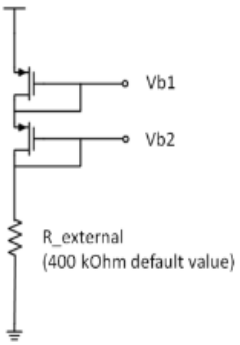

Figure 6: Bias Generation Circuit

It is important to note that the maximum current consumption per cell, including photocurrent and biasing current, is 8 μA. If necessary, the external resistor can be replaced with a different value to adjust the biasing current to a desired level.

2.1.4 Multiplexer & Shift Register

The 32:1 MUX (multiplexer) is a component that allows the selection of one out of 32 input channels and the routing of the selected channel to the output. In this specific case, the 32 channels are the 32 photodiodes integrated into the chip. The MUX is constructed by 32 CMOS switches(Figure 7) in parallel, where each switch corresponds

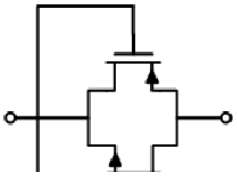

Figure 7: CMOS switch with digital gate control

to one channel. The switches are designed to have a low on-resistance, which is the resistance when the switch is turned on and conducting current. The lower the on-resistance, the less signal loss occurs when the switch is turned on.

The on-resistance of the switches is carefully designed to be around 300 Ohm at the middle biasing level, with a minimum of 180 Ohm and a maximum of 320 Ohm. This means that when a channel is selected, the switch connecting that channel to the output will have an on-resistance in the range of 180-320 Ohm, depending on the biasing level. The integrated MUX takes the data from the 32 channels and controls the release of the measured data to the microcontroller (µC) using a Shift Register. It allows for the selection of individual channels in a sequential manner. The shift register is a 32-bit register, with each bit corresponding to one channel of the MUX. By shifting in a 1 bit into the register, the corresponding channel is selected, and its measured data is passed through the MUX and onto the output. This enables the efficient collection of data from multiple channels, as only one channel is selected at a time. When a channel is selected, the measured data from that channel is passed through the switch and then to the output of the MUX, where it is then processed by the µC. The MUX enables efficient data collection from multiple channels with minimal signal loss.

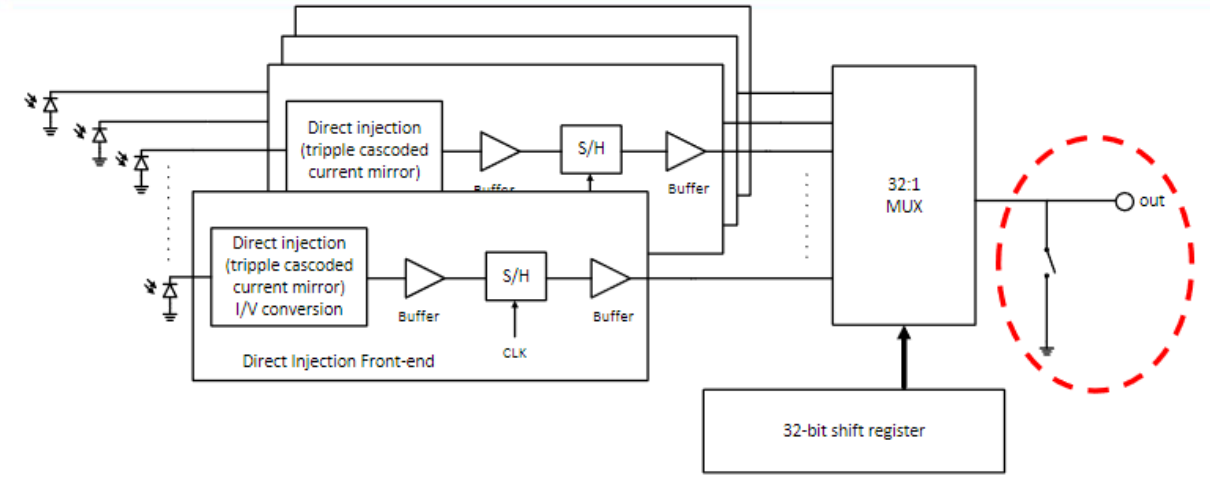

Figure 8: SR_reset_n Low Phase

2.2 NASIKA v2 and NASIKA v3

Building on the general ASIC structure described in the previous sections, this chapter will delve into the two specific versions of the photonic chip that offer flexibility in measuring a range of photodiode current values. This flexibility is achieved through modifications to the I/V conversion stage, which will be explored in detail below. In NASIKA v2, an integrated resistor is used, which converts the photocurrent to a voltage signal. The choice of the resistor is crucial as its noise contribution must be kept to a minimum. In this case, a 1 MOhm

resistor was selected because its noise contribution is negligible. The noise voltage of the resistor is determined by the Boltzmann constant, temperature, and resistance of the resistor. At a bandwidth of 10 kHz, the noise voltage is calculated to be 12 μVrms. However, at a higher bandwidth of 100 kHz, the noise voltage increases to 40.7 μVrms.

The minimum voltage that can be detected by the ASIC is determined by the product of the minimum detectable current and the resistance of the resistor. In this case, the minimum detectable current is 2 nA. Therefore, the minimum voltage that can be detected is calculated as Vmin=2nA x 1MOhm = 2 mV. This voltage is sufficiently large to provide a good signal-to-noise ratio for the photonic chip. The use of a 1 MOhm resistor ensures that the noise contribution is kept to a minimum, and the signal is reliably converted into a voltage that can be processed by the ASIC. This readout circuit enabled the readout of currents between 2uA to 2nA for a global clock frequency of up to 25kHz.

In NASIKA v3, the amount of charge a capacitor can store is proportional to its capacitance value. Therefore, by selecting an appropriate capacitance value, the I/V conversion circuit can be designed to amplify or detect very low-value currents. In the case of NASIKA v3, a capacitor value of 19.867pF is used. This readout circuit enabled the readout of currents between 2p to 2nA.

3 PCB Design

The integration of the ASIC into a complete measurement system requires a printed circuit board (PCB) that provides a physical interface between the ASIC and other components. To ensure proper connectivity and functionality, a custom footprint was created based on the size and layout of the ASIC. This footprint includes the locations of the bond pads, which are the small metal contacts on the surface of the ASIC that are used to connect it to the PCB.

To establish a connection between the ASIC and PCB, rebond wires are employed, which are thin wires that are bonded to the bonding pads on the ASIC and the corresponding pads on the PCB.

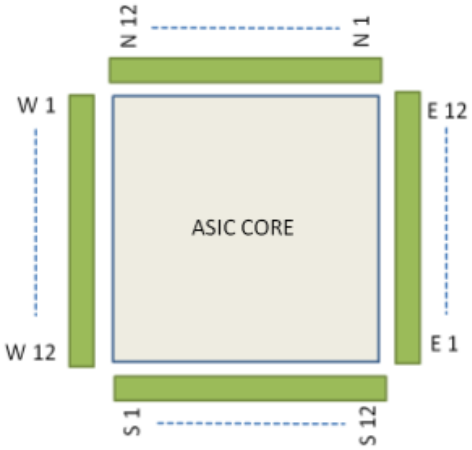

Figure 9: ASIC Pin Numbering Sequence

The PCB is typically designed to provide a secure and stable mounting platform for the ASIC, while also providing a means of connecting the ASIC to other components or circuitry. In this case, the ASIC is connected to 12x2 two-pin connectors, which are typically used to interface with other circuitry or components.

The ASIC has a total of 48 pads arranged in groups of 12 on each side(Figure 9) labeled PD<0> to PD<31> and are connected to the photodiode array block via the connector. There is also a supply pin that provides a voltage of 3.3V to power the ASIC. In addition, there are 4 clock signal pins that provide clock signals to the ASIC for proper timing of the operations(described later).

There is a digital supply and ground pin for powering the digital circuits within the ASIC, as well as a substrate pin. The VDD3 supply is used to power the ESD structures in the padring, which protect the ASIC from electrostatic discharge.

The ASIC PCB is designed without a common ground plane. This is done because the ASIC contains both digital and analog components, and separating the grounds helps to minimize noise and interference between them. Also, in the areas where the ASIC and rebond wires are placed, the solder mask is removed to allow direct contact between the bonding pads on the ASIC and the rebond wires. Solder mask is a protective layer on a printed circuit board (PCB) that prevents solder from flowing to unintended areas during the soldering process. This is necessary for proper electrical connections to be made between the ASIC and the external circuitry. If the solder mask were left in place, it would prevent the rebond wires from making contact with the bonding pads, leading to faulty connections and potentially causing the circuit to not function properly.

Figure 10 illustrates the 3D view of the PCB Design in KiCAD & the subsequent manufactured PCB.

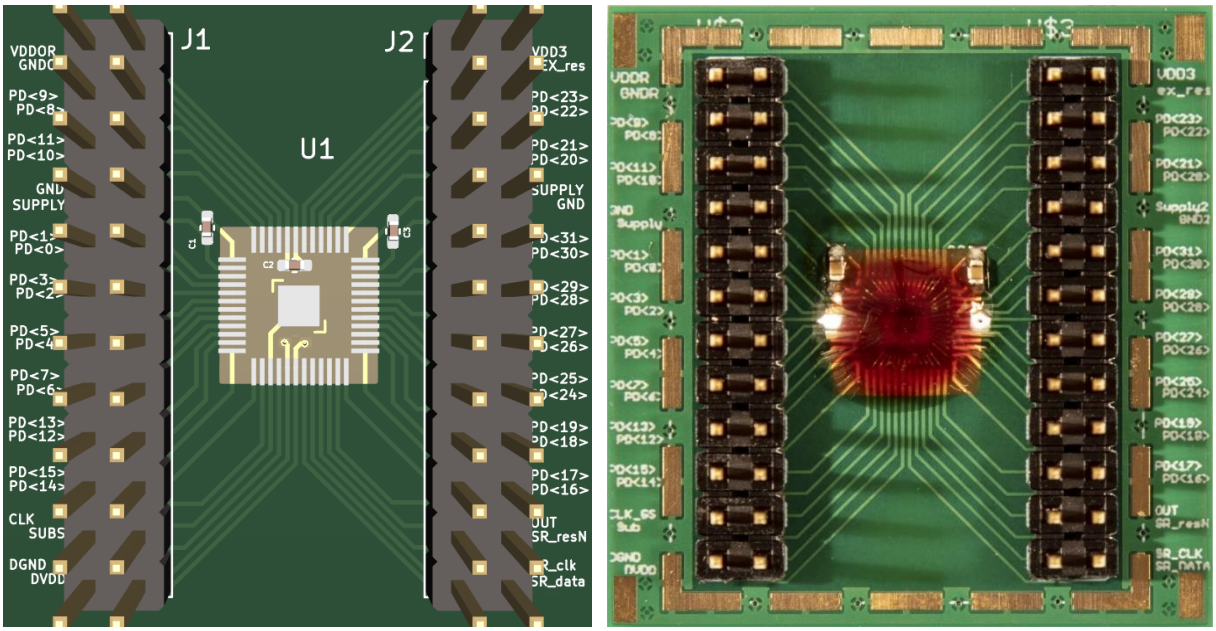

Figure 10: PCB Layout in KiCAD and the manufactured PCB

4 Control of Clock Signals

The Clock Signals plays a crucial role in the control of the ASIC's operation. By providing four synchronized pulses(Figure 11) to all 32 front-end circuits, the CLK signal enables simultaneous signal sampling and holding. This ensures that all channels are sampled at the same instant, providing accurate measurements. The frame rate, which is the rate at which signals are read out, is determined by the speed of the CLK signal. By adjusting the frequency of the CLK signal, the frame rate can be modified to suit the specific measurement requirements.

Once the signals are stored on the capacitors and have settled, they can be read out using the 32:1 MUX which is controlled by the shift register, which allows only one channel to be selected at a time. By going through 32 clock cycles, all the channels can be read out in sequence.

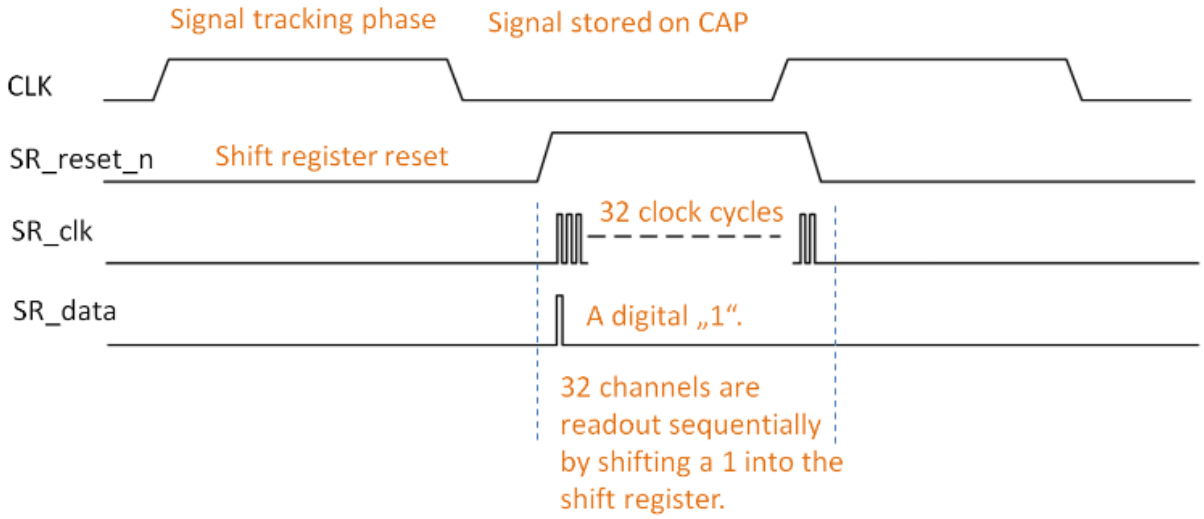

Figure 11: Digital Control Timing Diagram

The digital control scheme is flexible, allowing the CLK frequency to be adjusted to achieve different frame rates. The duty cycle of the CLK signal does not necessarily need to be 50%, meaning that the high and low states of the signal don't need to be equal in duration.

It's suggested to reset the shift register before reading new frame data, which ensures that the data is properly synchronized with the clock signal. The shift register clock is rising-edge active, meaning that it registers the input data on the rising edge of the clock signal. To

operate the shift register correctly, the SR_data signal should be slightly earlier than the SR_clk rising edge, so that the data is registered at the correct time.

5 Simulation of ASICs using a Testbench in Cadence Virtuoso

In order to ensure the functionality and performance of the ASIC, it is necessary to conduct thorough testing before fabrication. One of the key steps in this testing process is the simulation of the ASIC using a testbench in software tools like Cadence Virtuoso. This allows for the evaluation of the ASIC's behavior under various operating conditions and the optimization of its design before physical implementation.

In this simulation environment, the clock signals used to drive the circuit are generated in a testbench. To generate clock signals, a voltage source is used to create a square wave with a specified period, pulse width, and delay. The detailed blocks are described below.

By simulating the clock signals(Figure 12) in the testbench with appropriate pulse width, delay, and period, the behavior of the ASIC can be analyzed and optimized for different operating conditions. This allows for the identification and correction of any potential issues with the design before the ASIC is fabricated and tested in the lab.

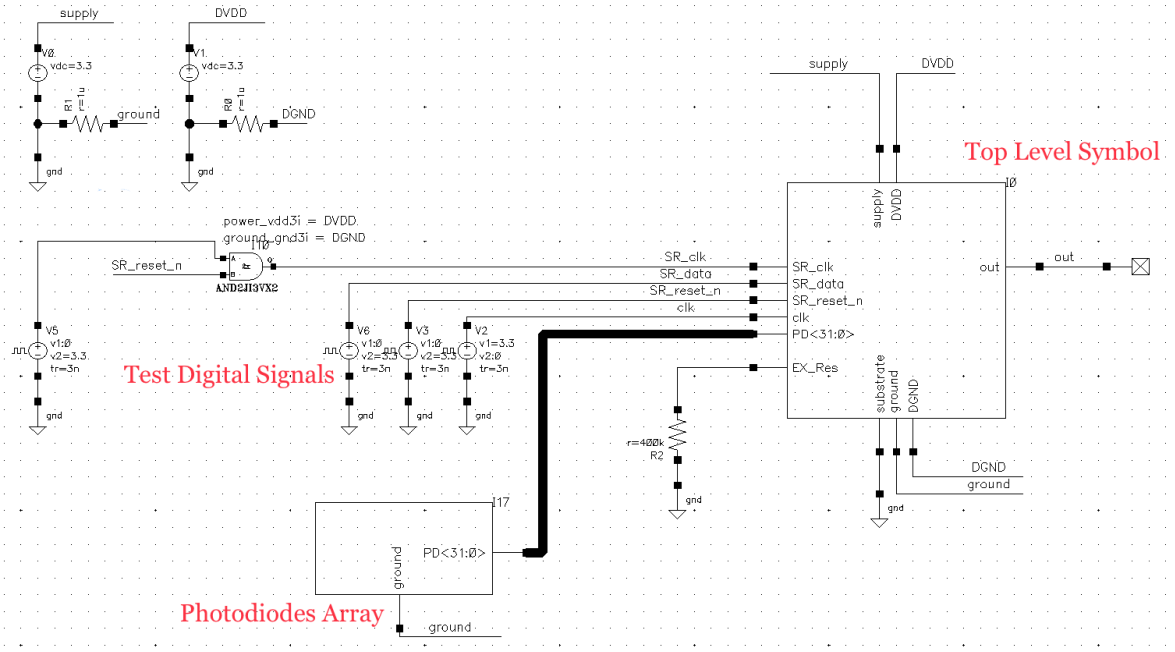

Figure 12 Testbench of the Schematic in Cadence Virtuoso

5.1 NASIKA v2 & v3

As shown in Figure 13, the photodiode array block consists of multiple photodiodes that are connected in parallel to the core readout block. Each photodiode produces a photocurrent that is proportional to the incident light on the photodiode.

The core readout block(Figure 14) contains current mirror, output buffer & the bias generation circuit.The shift register block is responsible for sequentially selecting the output of each photodiode in the array and passing it to the multiplexer.

The multiplexer selects the output of one photodiode at a time and passes it to the core readout block for processing. The clock signals in the testbench are used to control the operation of the shift register and multiplexer, ensuring that the output of each photodiode is selected and processed in the correct order.

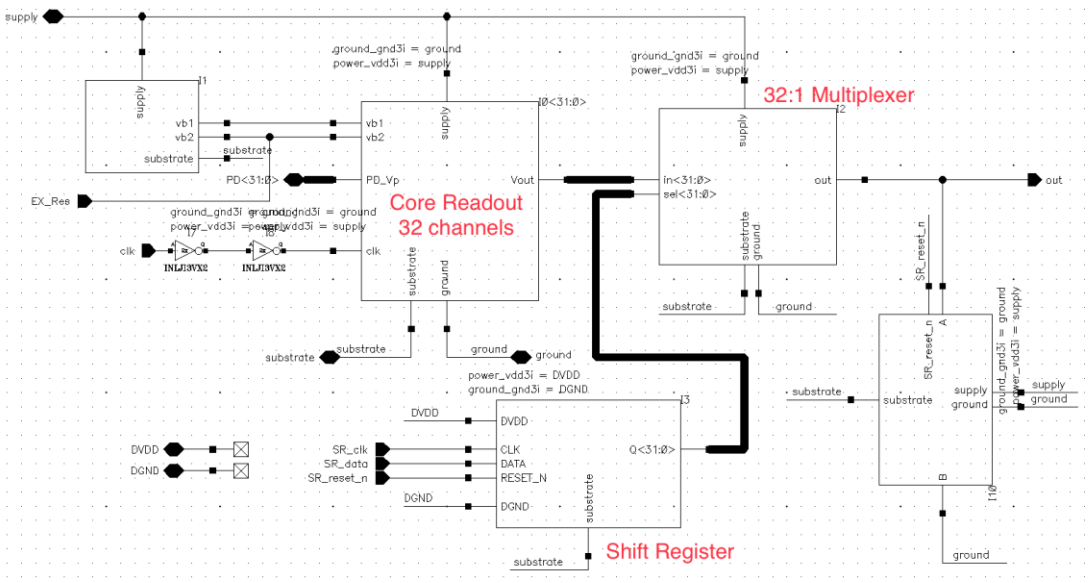

Figure 13 ASIC Schematic for NASIKA v2

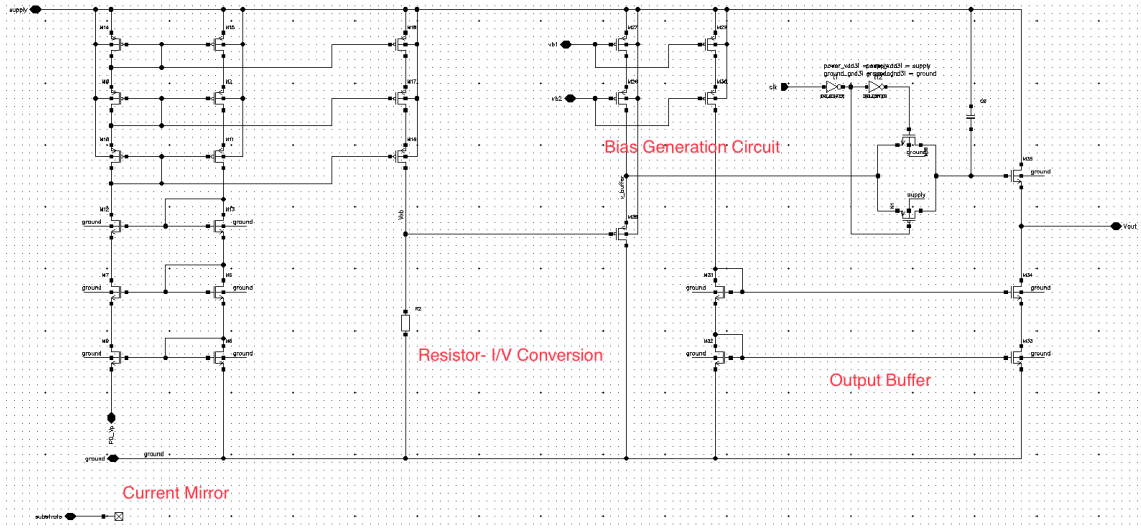

Figure 14 Readout Block for NASIKA v2

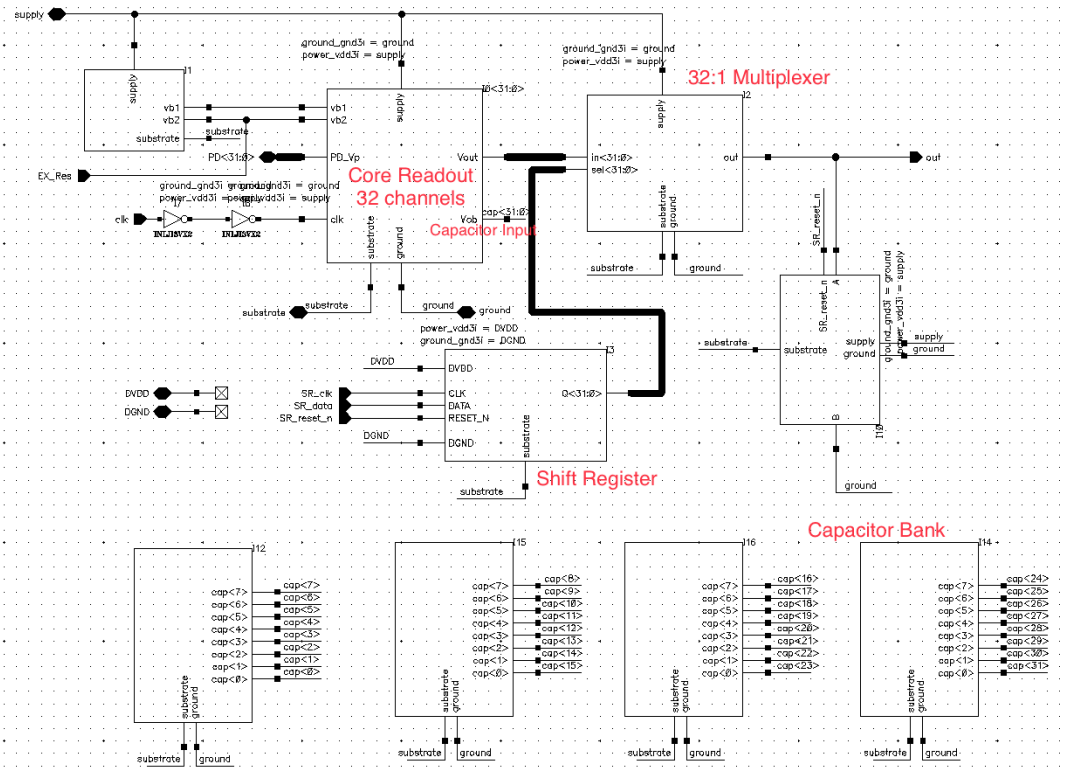

Figure 15 ASIC Schematic for NASIKA v3

The test bench in both v2 and v3 is similar, as the overall functionality of the ASIC is the same in both cases. However, the specific parameters used in the test bench, such as the pulse width, delay, and period of the clock signals, are depending on the specific design and

operating range of each version of the ASIC. The major difference between them is in the core readout circuit of v3(Figure 15), where a capacitor bank of 32 capacitors is connected for I/V (current to voltage) conversion whereas in v2(Figure 13), a resistor is used.

5.2 Simulation Results Analysis- Similarities & Differences between NASIKA v2 and NASIKA v3

As previously mentioned, the fundamental purpose of the photonic chip remains consistent across both versions. As a result, the output results exhibit a comparable pattern. Nevertheless, since these chips are intended to function within distinct input current ranges, minor circuit differences give rise to certain distinctions. The subsequent section delves into both these points in detail.

5.2.1 Similarities

Both versions of NASIKA exhibit a similar pattern in their output results, which resembles a staircase. This can be attributed to the current-to-voltage conversion and sampling process employed in the readout circuit. In response to incident light, each photodiode produces a photocurrent, which is then transmitted to the readout branch through the current injection unit.

The current-to-voltage conversion stage converts the photocurrent into a voltage signal, which is then buffered and sampled simultaneously for all 32 channels, which is referred to as a global shutter function. However, since the voltage is sampled at discrete intervals, the resulting output signal will have a stair-step pattern. This is because the voltage value is held constant between each sampling point and jumps to the next level at the next sampling point. The magnitude of the voltage is proportional to the amount of photocurrent generated by the photodiode during the sampling interval.

So, if the photocurrent generated by the photodiode increases in a stepwise manner, for example, due to increasing the intensity of the incident light in steps, the voltage signal will also increase in a stepwise manner.

As a result, when the reset switch is activated, the voltage on the buffer component drops rapidly, but does not drop to zero immediately due to the residual charge. The resulting minor fluctuation range at the end of each sample step is a reflection of this residual voltage.

As shown in Figure 16 & as mentioned before, the clock signals are essential in the operation of the ASIC as they provide the necessary timing for the different circuit elements to perform their functions. The period of the clock signal determines the frame rate of the circuit which

is the CLK signal in the figure. A shorter period results in a higher frame rate, which means the circuit can sample and read out the signals more frequently.

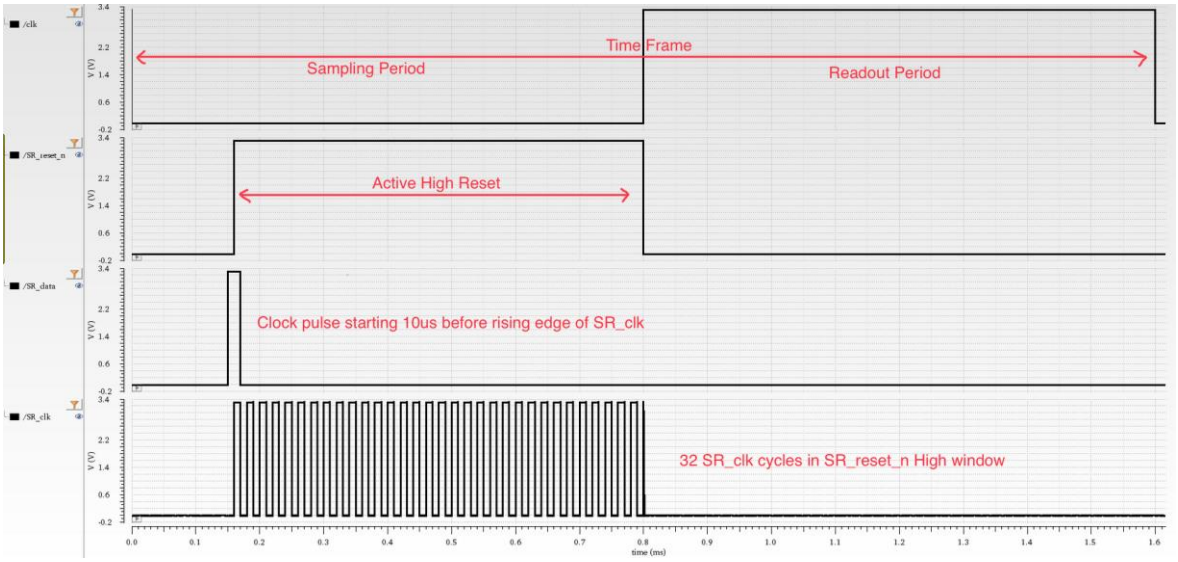

Figure 16 Simulated testbench clock signals

5.2.2 Differences

In NASIKA v2, a resistor is used in the I/V conversion stage, which converts the photocurrent into a voltage signal that is then buffered and sampled. This design can measure photocurrents ranging from 2uA to 2mA (Figure 18), and it has been observed that it can maintain a linear sampling period in the output signal up to a sampling frequency of 25kHz.

Figure 16 shows simulated 4 clock signals along with its ouput voltage with a readout period of 800us. As can be observed here and discussed earlier, the staircase pattern of the output is maintained(Figure 19). Figure 20 with a readout period of 100us exhibits the same pattern thus stazing within the operating range. It can also be observed from output results for both frequencies in Figure 17 and Figure 20, that the use of a resistor in the I/V conversion stage

here results in a fixed gain, which means that the output voltage remains constant regardless of the frequency ranging from 1.6V to 0.5V approximately.

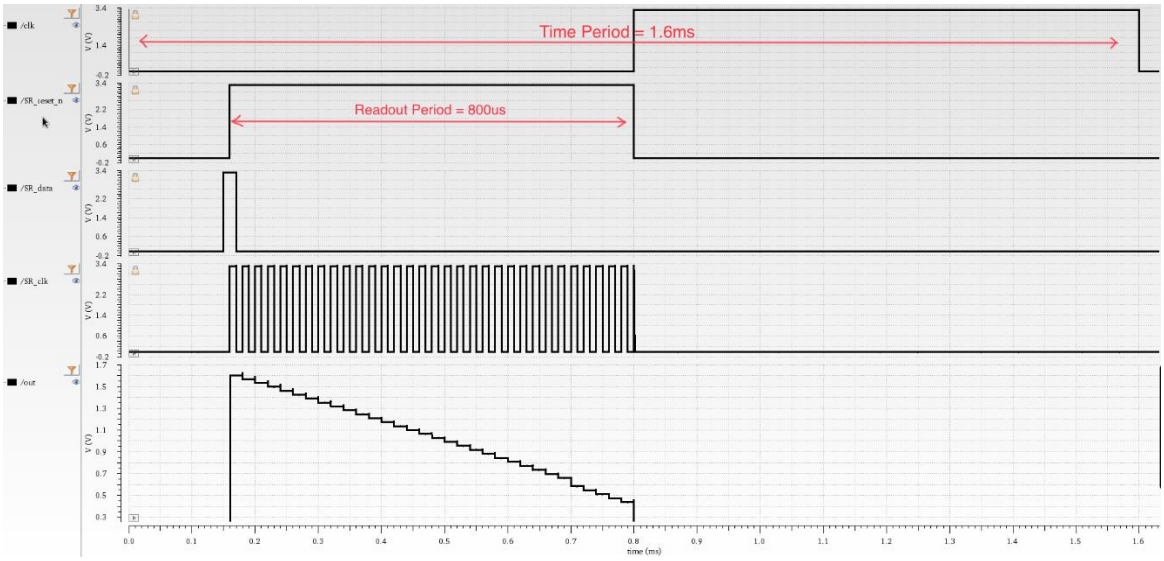

Figure 17 Simulated clock signals for CLK Period 1.6ms

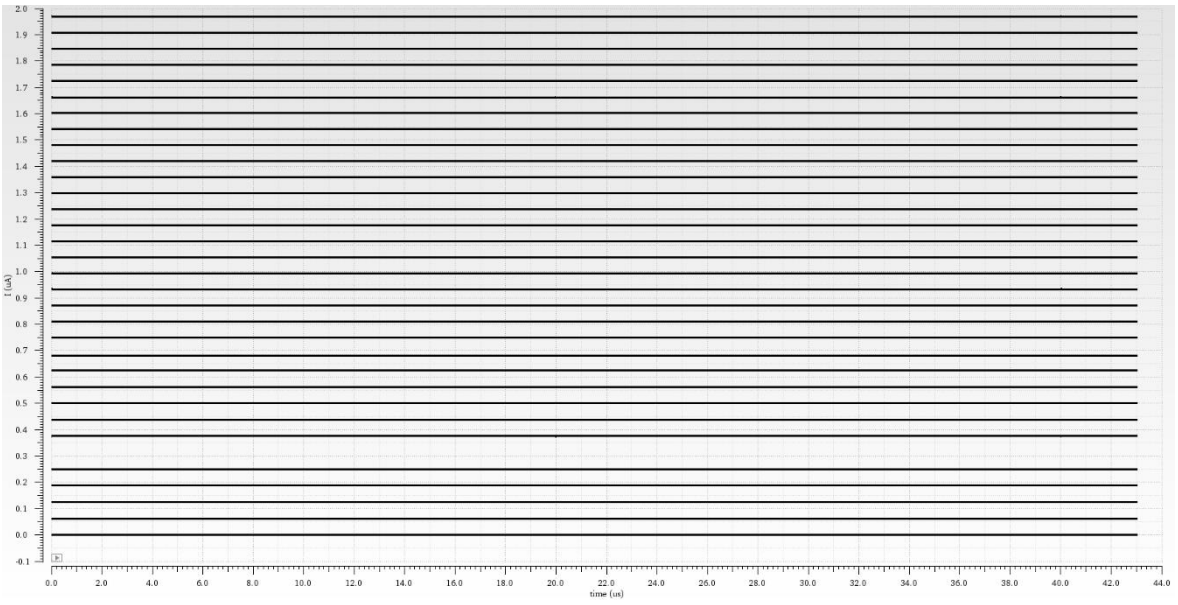

Figure 18 Photodiode Currents

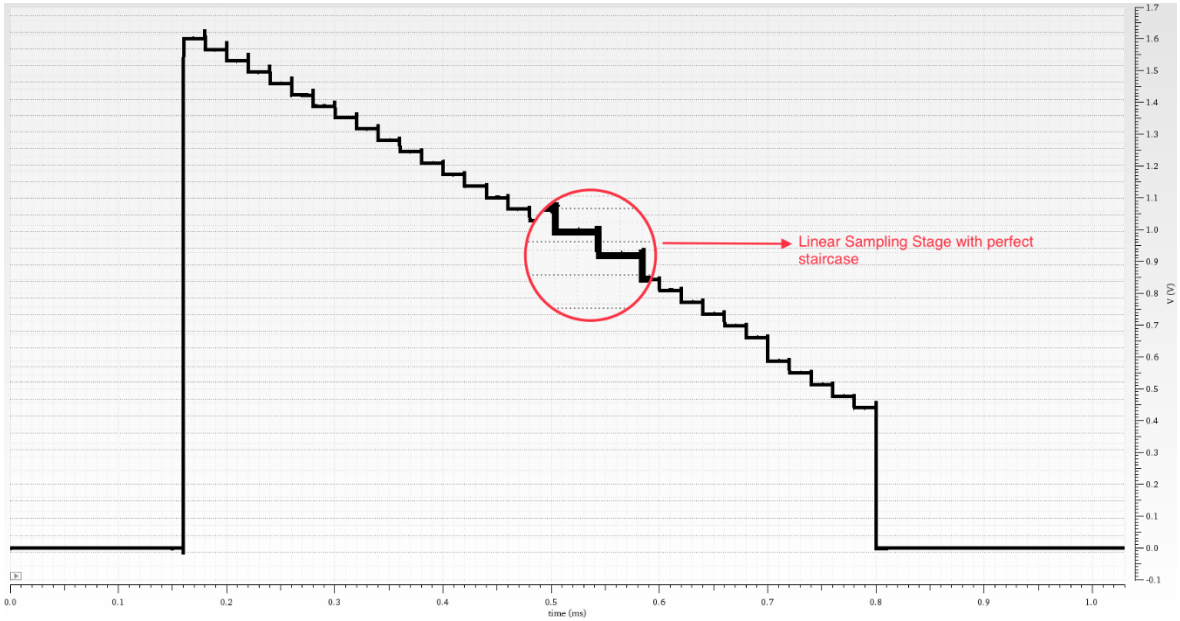

Figure 19 Zoomed Output Voltage for 1.6ms CLK period

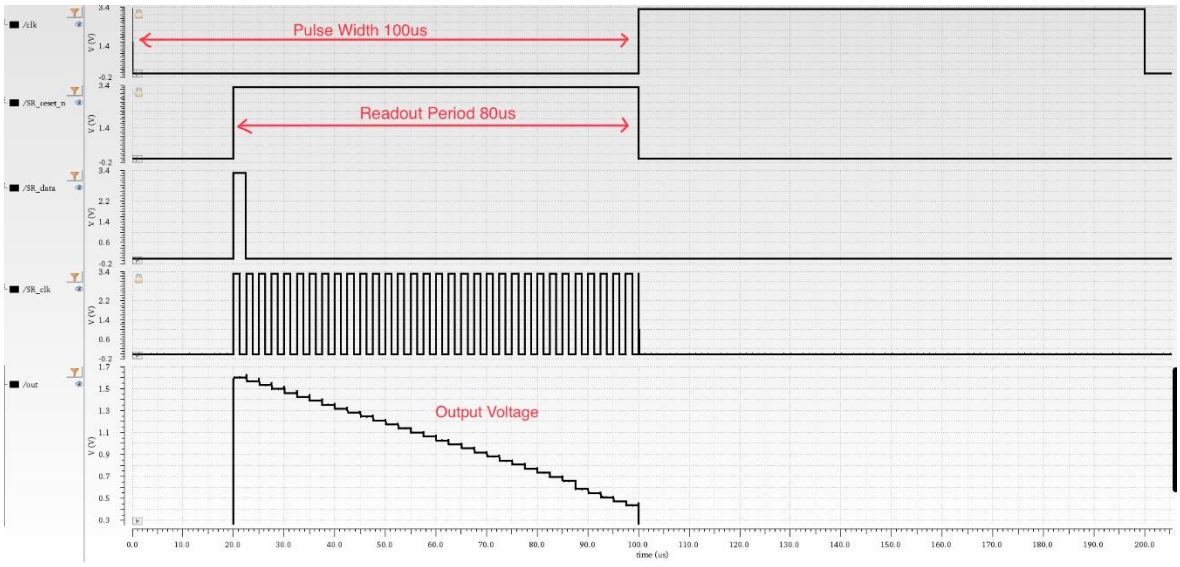

Figure 20 Simulated clock signals for CLK Period 0.2ms

Figure 21 Output Voltages for CLK Period 40us

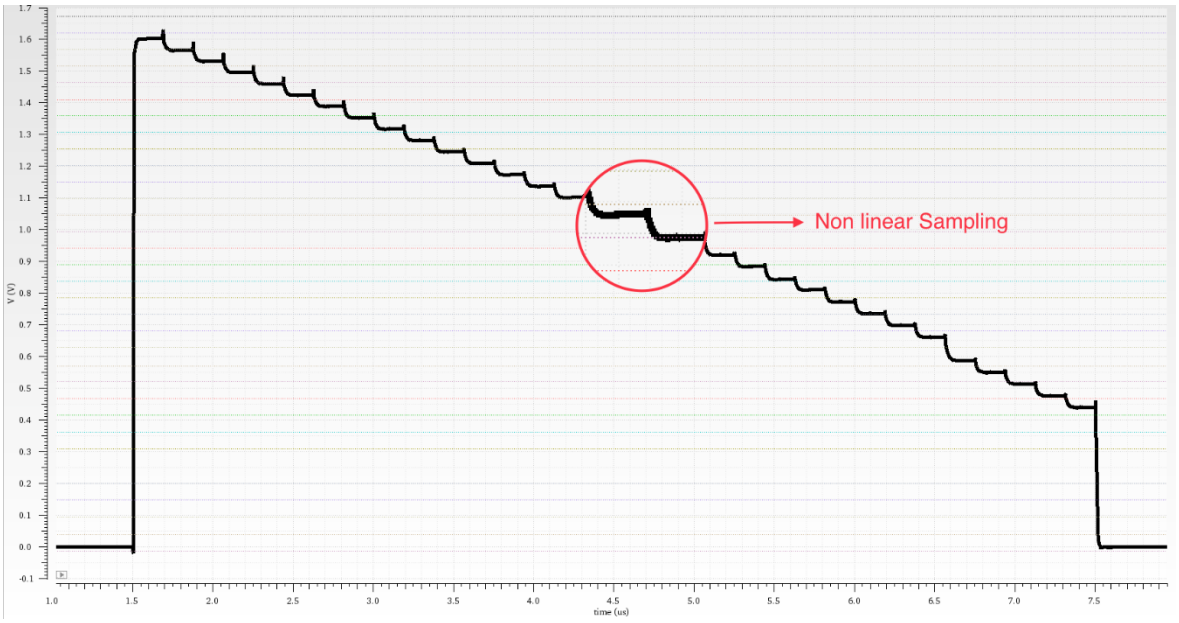

Figure 22 Output Voltages for CLK Period 15us

However, when the ASIC is simulated from a frequency of 25kHz(CLK Period 40us; Figure 20), the linear nature of the sampling period is distorted. When the CLK period is increased to 15us(Figure 22), the output voltages no longer follow a linear pattern & are completely distorted. It should be noted however that the value of the output voltages still remain the same, with the distortion only caused during the sampling period. It can be inferred that, the faster the readout period is, the time available for settling between sample steps is reduced.

This can cause the ASIC to not settle to their steady-state values, resulting in a curved or sloped shape at the corners of the horizontal sample line.

However, in NASIKA v3, a capacitor is used in the I/V conversion stage instead of a resistor. This design can measure smaller photocurrents ranging from 2pA to 2nA, and can operate at a lower frequency range of 50kHz to 10Hz & lower. The use of a capacitor in the I/V conversion stage allows for a higher gain and a lower noise floor, which is important for measuring very small photocurrents.

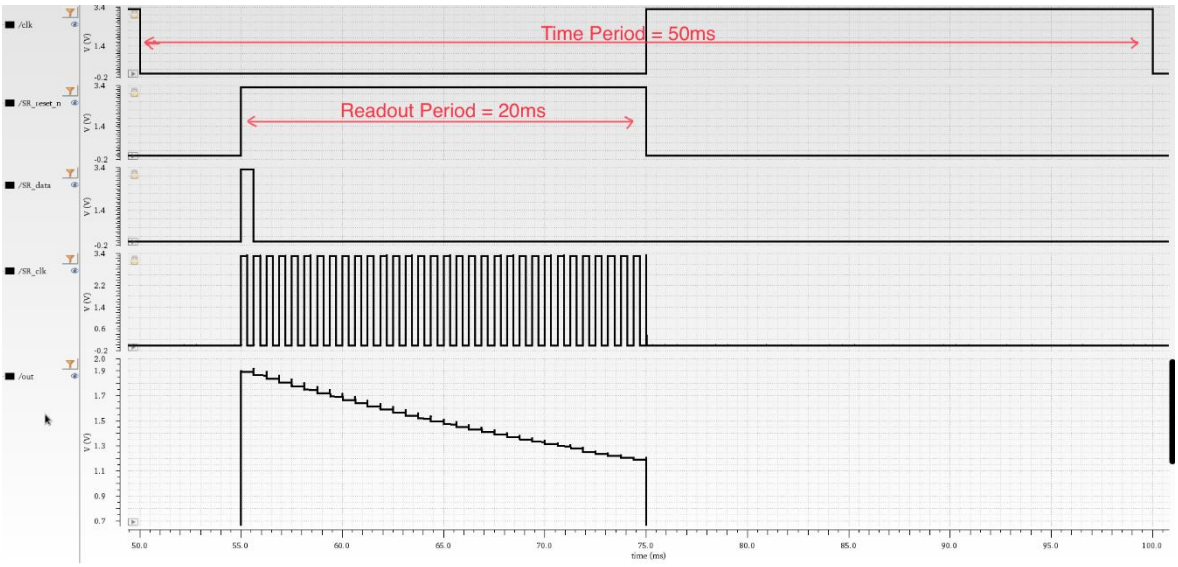

Figure 23 Simulated clock signals for CLK Period 50ms

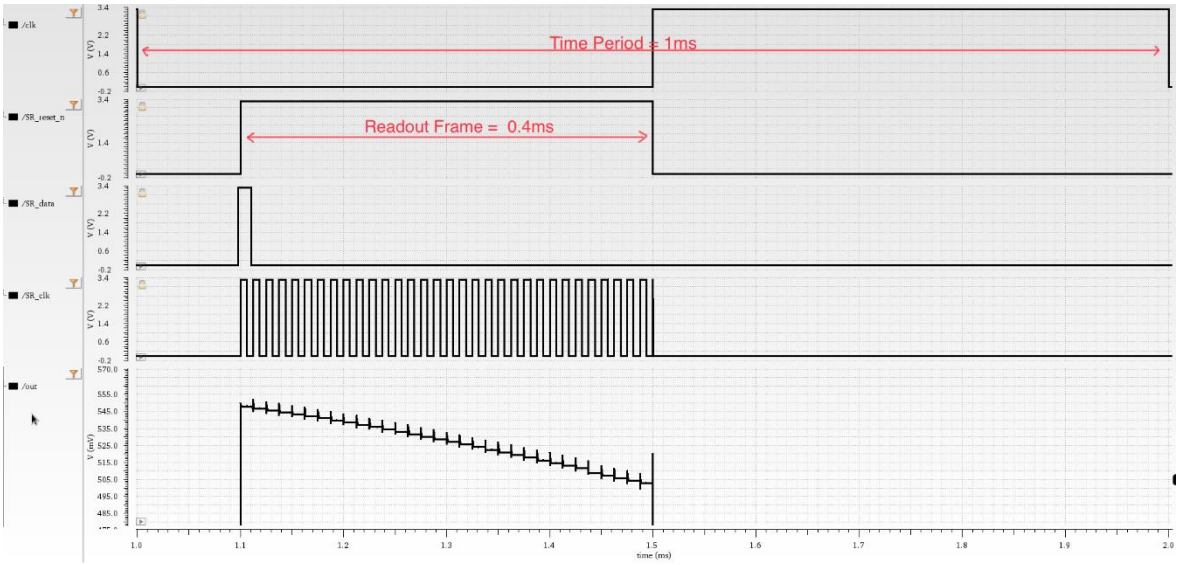

Figure 24 Simulated clock signals for CLK Period 1ms

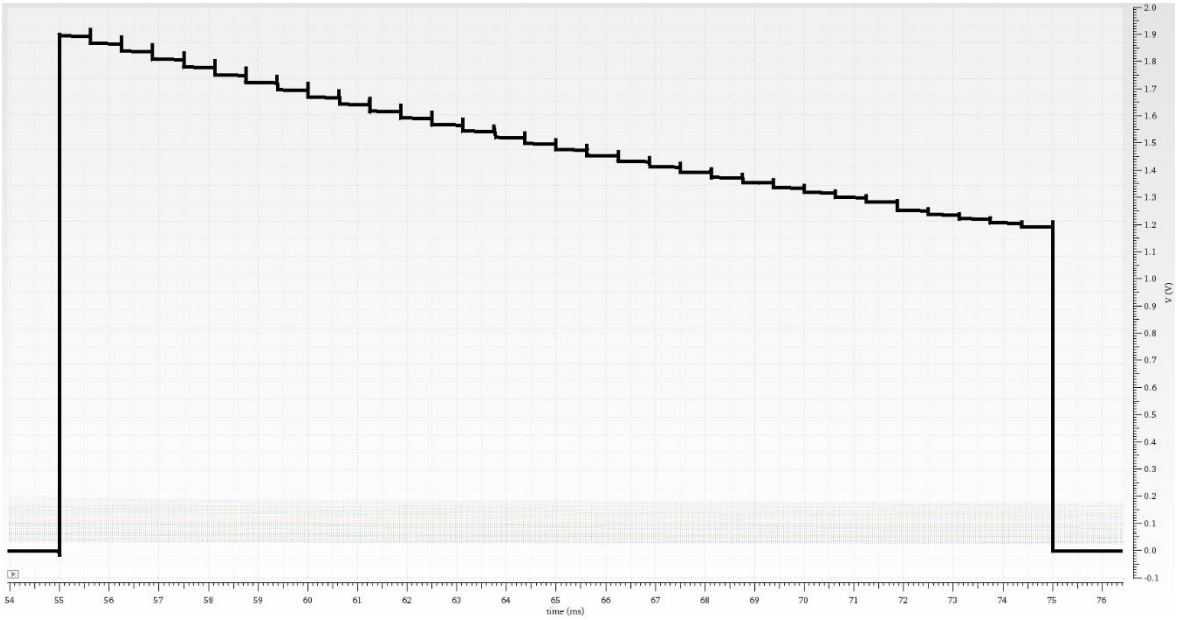

Figure 25 Output Voltages for CLK Period 50ms

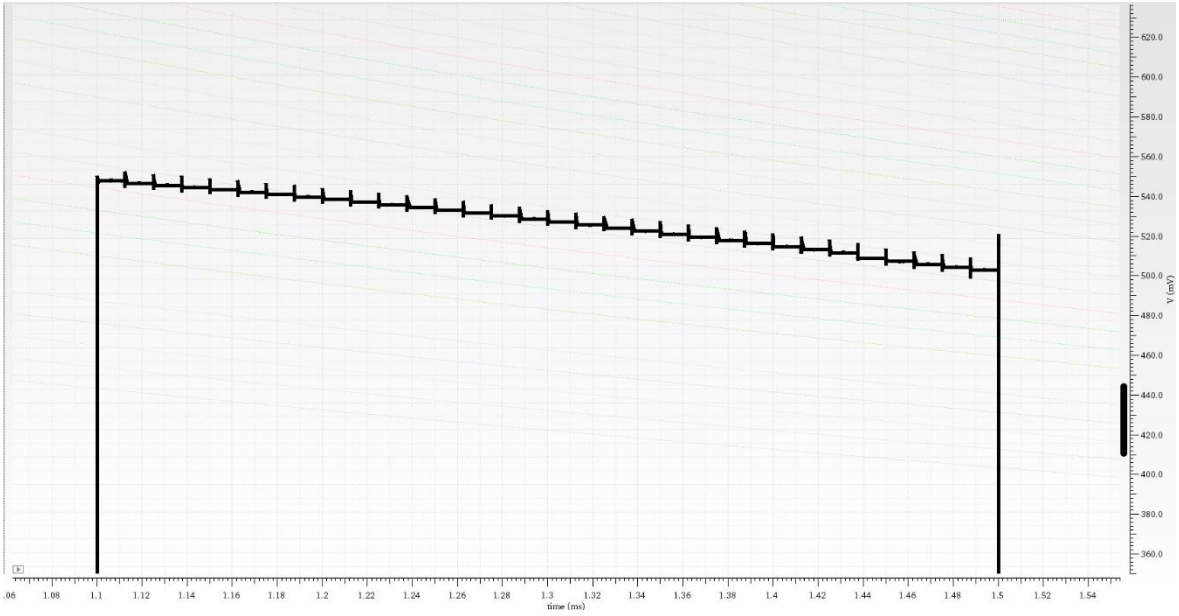

Figure 26 Output Voltages for CLK Period 1ms

Figure 23 & 25 shows a simulated result with integration time of 50ms (Frequency 20Hz). The output follows the same staircase pattern as discussed in v2 as stays within the operating range. When compared to the output in Figure 24 & 26, the pattern is still the same but it can be seem that the output voltage values are no longer constant with changing frequency. This is because in contrast to v2, v3 uses a capacitor in the I/V conversion stage, which acts as an integrating element. The output voltage in this case is proportional to the integrated photocurrent, and the integration time is determined by the capacitance value. As the

frequency decreases, the integration time increases, resulting in a larger integrated voltage and thus a higher output voltage value. Therefore, in v3, the output voltage values increase with decreasing frequency (i.e., increasing capacitor integration time).

As shown in Figure 27, when the CLK frequency is further increased to 50kHz, the sampling period no longer is linear as same as shown in v2. However, it can also be observed that the fluctuation of voltage values at the end of every sample step is also greater than measured at previous frequencies. Normally, the small fluctuation is caused by the reset switch that discharges the residual voltage on the buffer. When the reset switch is activated, it quickly discharges the remaining voltage on the buffer component, causing the output voltage to drop to a low level. However, the voltage on the buffer component cannot be discharged instantaneously due to the finite capacitance or resistance of the buffer component. With increasing frequencies, the duration between consecutive samples becomes shorter, which reduces the time available for the capacitor to charge and discharge. This increases the amount of residual voltage stored on the buffer thus leading to higher fluctuations than at lower frequencies.

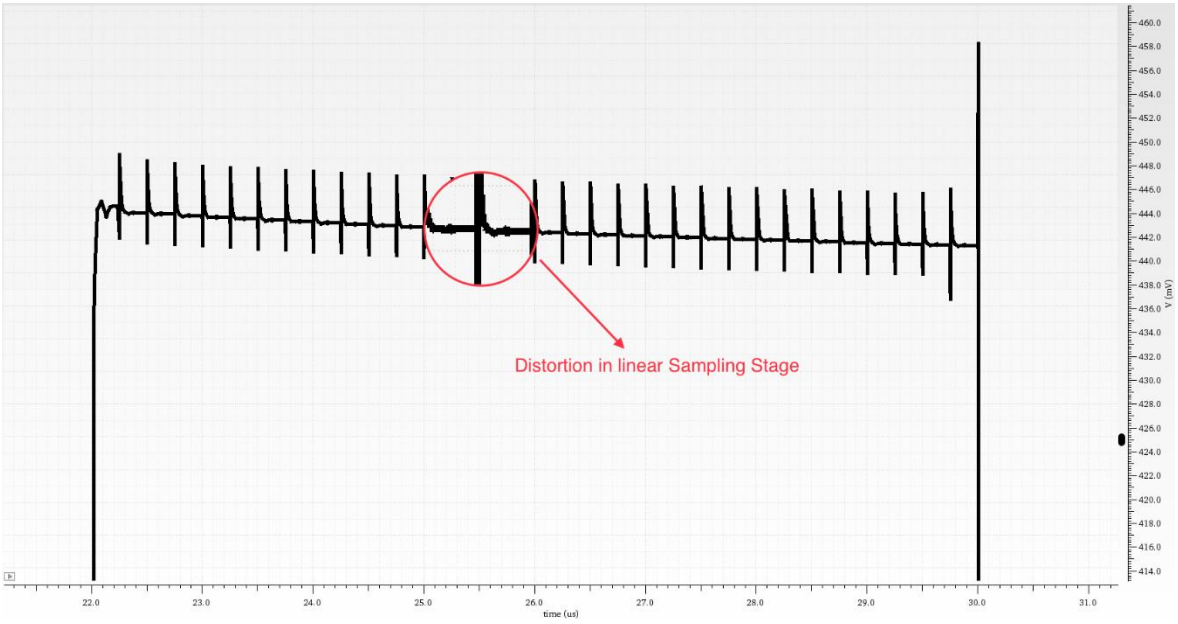

Figure 27 Output Voltages for CLK Period 20us

6 Microcontroller Programming

The ASIC described here incorporates a microcontroller integrated on the board, which functions as the central controller to enable readability of output. The microcontroller is responsible for generating the clock signals for the shift register of the ASIC to read data from the photodiodes and generate other subsequent clock signals. Additionally, the microcontroller converts the measured data into digital values using the integrated ADC and stores them in a buffer memory.

The microcontroller selected for this system is the MSP430F5529 from Texas Instruments(Figure 28), which is a powerful microcontroller with a wide range of features and capabilities. It is programmed with specific software to carry out the aforementioned tasks effectively. Furthermore, the microcontroller controls a UART interface that facilitates the transfer of data between a computer and the spectrometer.

To enable serial communication and programming of the microcontroller, a TI MSP-EXP430F5529LP launchpad is utilized. This device provides a convenient and user-friendly interface(Code Composer Studio-CCS) for programming and debugging the microcontroller. Hardware equipment used to facilitate this setup include jumpers for

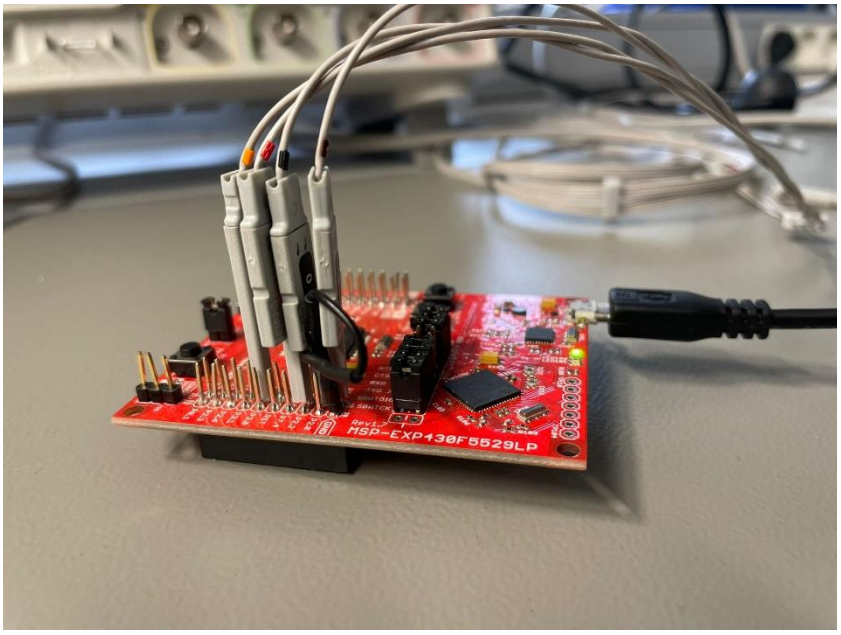

Figure 28 MSP430F5529 Microcontroller Setup

configuration and additional peripheral elements, such as oscillators and a power supply(Figure 29).

In summary, this system is a well-designed and efficient spectrometer that utilizes a powerful microcontroller to control and manage its various functions. The use of the MSP430F5529 microcontroller, in combination with the ASIC and other peripheral elements, allows for accurate and reliable measurements to be made, while the UART interface enables seamless data transfer between the spectrometer and a computer.

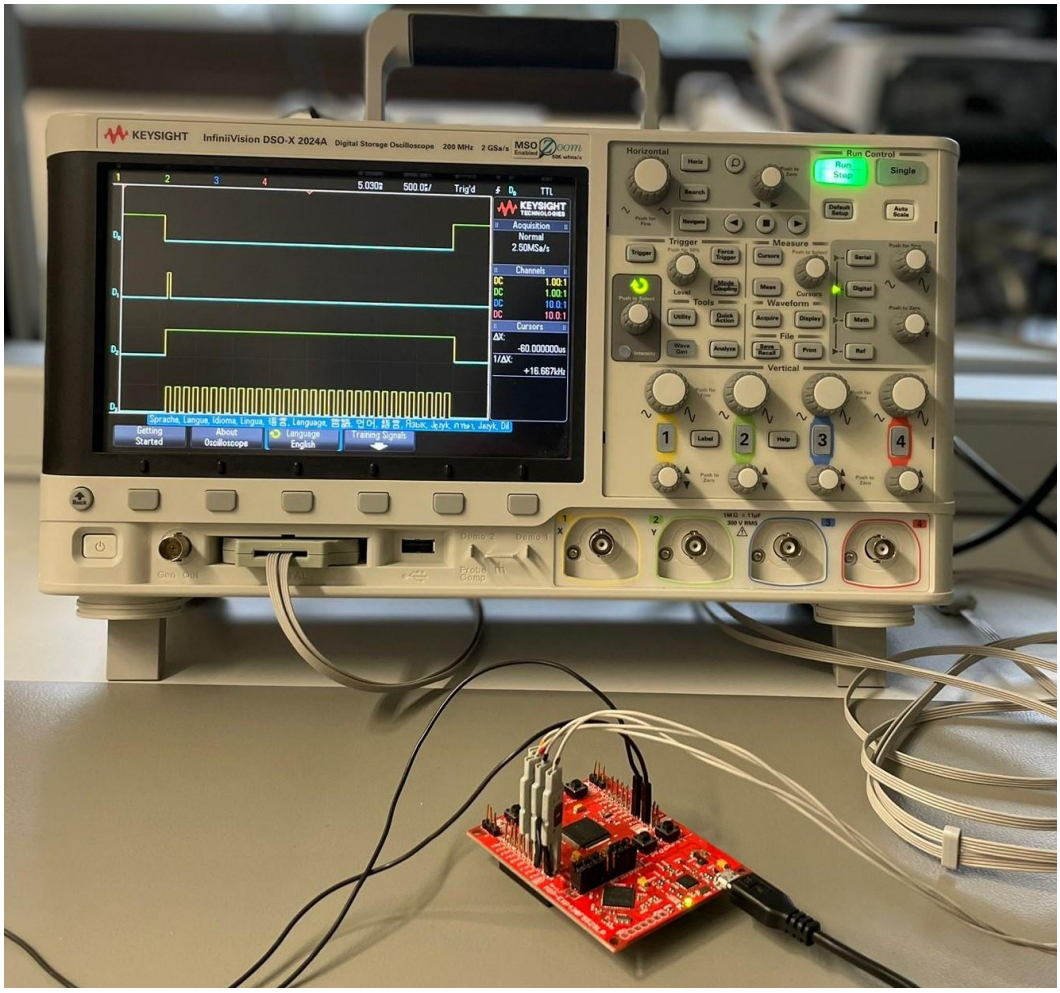

Figure 29 Measurement Setup for Control Signals and Output Waveforms

6.1 Photocurrent Readout Using ADC

Here, the measured output values obtained from the ASIC are transferred to the MSP430F5529 microcontroller's integrated ADC after every complete cycle of the SR_clk Signaö. The ADC operates using the Successive-Approximation-Register (SAR) principle and has a resolution of 12 bits, as specified in the microcontroller's datasheet. It is worth

noting that the ASIC documentation suggests that a 12-bit resolution is more than sufficient, as the measured data needed for this system only has a resolution of 10 bits.

After the conversion process, the photocurrent values are stored in a FIFO buffer memory. This buffer memory is organized in a First-In First-Out (FIFO) fashion, meaning that the data stored first is retrieved first. This arrangement allows for efficient data storage and retrieval, which is essential for the system's overall performance.

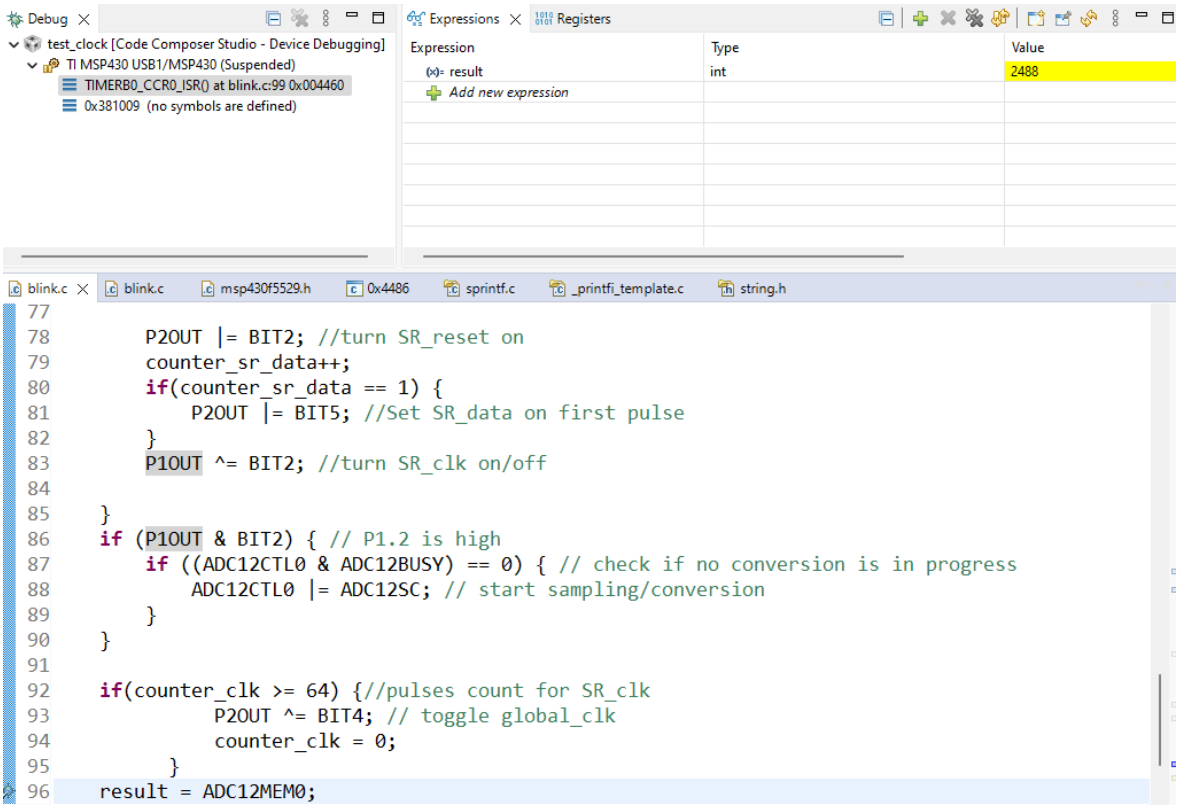

Figure 30 ADC Ouput on CCS

Figure 30 shows an example of the ADC sampling the measured values from the GPIO Pin that outputs SR_clk and proceeding to storing the value in a buffer memory(shown in the variable “result”). The detailed code for the above mentioned application can be found in the Appendix.

7 Conclusion

The main objective of the project was to study and analyze the control signals for the SiGe photodiode developed in the NASIKA joint project. A simulation was setup in Cadence Virtuoso and the MSP430F5529 microcontroller was utilized to generate the required clock signals for the ASIC and read out the output voltages.

During the course of the thesis, the simulation data for both versions of the photonic chip was comprehensively analyzed. Additionally, a μC-software was developed to control the ASIC and process the measured data.

The subsequent steps in the project will involve transferring the acquired measurement data to a graphical user interface through a serial interface. This will enable efficient data storage and retrieval and facilitate the complete commissioning of the spectrometer.

Additionally, the ADC readout of both versions of photonic chips can be further explored. It was noted that both chips have limitations in operating frequencies, resulting in non-linear sampling in the output graph. To address this issue, one possible solution is to delay the start of the ADC readout until the circuit components have settled to their steady-state values. This approach allows more time for settling, resulting in a more accurate and stable output signal. Delaying the ADC readout effectively shifts the sample points on the output graph, resulting in a linear output graph with improved accuracy and range. However, it is crucial to optimize this delay to balance settling time and maximum clock frequency to ensure accurate measurements at the desired sampling rate.

8 Appendix

Code to generate control clock signals on MSP430F5529 microcontroller

```
#include <msp430.h>
#include <stdio.h>

unsigned int counter_clk = 0;
unsigned int counter_sr_data = 0;
int result;


void main(void) {
  WDTCTL = WDTPW + WDTHOLD; // Stop watchdog timer

  // Configure GPIO pins
  P1DIR |= BIT2;                          // SR_clk
  P2DIR |= BIT2 | BIT4 | BIT5;            //SR_data- P2.5, SR_reset_n- P2.2, global_clk- P2.4

  ADC12CTL0 = ADC12SHT02 + ADC12ON;       // Sampling time, ADC12 on
    ADC12CTL1 = ADC12SHP;                 // Use sampling timer
    ADC12IE = 0x01;                       // Enable interrupt
    ADC12CTL0 |= ADC12ENC;
    P6SEL |= 0x01;                        // P6.0 ADC option select

  // Configure TimerB0
  TB0CCR0 = 0;
  TB0CCTL0 = CCIE;                        // Set-reset output mode
  TB0CTL = TBSSEL__SMCLK + MC__UP + TBCLR; // Set clock source to SMCLK and count up mode
  _enable_interrupt();
  TB0CCR0 = 5 - 1;                        // Set period
  while(1){
  }
}

#pragma vector = TIMER0_B0_VECTOR
__interrupt void TIMERB0_CCR0_ISR(void)
{
    P2OUT &= ~BIT5;                       //SR_data always off unless triggered
    counter_clk++;
    if(P2OUT & BIT4) {                    // check if GLOBAL_CLK is ON
        P1OUT &= ~BIT2;                   // turn SR_clk off
        P2OUT &= ~BIT2;                   // turn SR_reset off
        counter_sr_data = 0;              //reset counter for SR_data
    }
    else {
        P2OUT |= BIT2;                    //turn SR_reset on
        counter_sr_data++;
        if(counter_sr_data == 1) {
            P2OUT |= BIT5;                //Set SR_data on first pulse
        }
        P1OUT ^= BIT2;                    //turn SR_clk on/off
    }
    if (P1OUT & BIT2) {                   // P1.2 is high
        if ((ADC12CTL0 & ADC12BUSY) == 0) { // check if no conversion is in progress
            ADC12CTL0 |= ADC12SC;         // start sampling/conversion
        }
    }
    if(counter_clk >= 64) {               //pulses count for SR_clk
              P2OUT ^= BIT4;              // toggle global_clk
              counter_clk = 0;
          }
    result = ADC12MEM0;

}
```

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